IM2G16D3FDB
2Gbit DDR3 SDRAM
8 BANKS X 16Mbit X 16

Ordering Speed Code	- 15E	- 125	- 107
	DDR3-1333	DDR3-1600	DDR3-1866
Clock Cycle Time ($t_{CK5,\ CWL=5}$)	3.0ns	3.0ns	3.0ns
Clock Cycle Time ($t_{CK6,\ CWL=5}$)	2.5 ns	2.5 ns	2.5 ns
Clock Cycle Time ($t_{CK7,\ CWL=6}$)	1.875 ns	1.875 ns	1.875 ns
Clock Cycle Time ($t_{CK8,\ CWL=6}$)	1.875 ns	1.875 ns	1.875 ns
Clock Cycle Time ($t_{CK9,\ CWL=7}$)	1.5 ns	1.5 ns	1.5 ns
Clock Cycle Time ($t_{CK10,\ CWL=7}$)	1.5 ns	1.5 ns	1.5 ns
Clock Cycle Time ($t_{CK11,\ CWL=8}$)	-	1.25 ns	1.25 ns
Clock Cycle Time ($t_{CK12,\ CWL=8}$)	-	-	1.25 ns
Clock Cycle Time ($t_{CK13,\ CWL=9}$)	-	-	1.07 ns
System Frequency ($f_{CK\ max}$)	667 MHz	800 MHz	933 MHz

Specifications

- Density : 2Gbits
- Organization :
  - 16M words x 16 bits x 8 banks (IM2G16D3FDB)
- Package :
  - 96-ball FBGA for x16
  - Lead-free (RoHS compliant) and Halogen-free
- Power supply : VDD, VDDQ = 1.35V (1.283V to 1.45V)
  - Backward compatible to VDD, VDDQ = 1.5V ± 0.075V
- Data rate : 1333Mbps / 1600Mbps / 1866Mbps
- 2KB page size for x16
  - Row address: A0 to A13 (IM2G16D3FDB)
  - Column Address: A0 to A9
- Eight internal banks for concurrent operation
- Burst lengths (BL) : 8 and 4 with Burst Chop (BC)
- Burst type (BT) :
  - Sequential (8, 4 with BC)
  - Interleave (8, 4 with BC)
- $\overline{\text{CAS}}$ Latency (CL) : 6, 7, 8, 9, 10, 11, 13
- $\overline{\text{CAS}}$ Write Latency (CWL) : 5, 6, 7, 8, 9
- Precharge : auto precharge option for each burst access
- Driver strength : RZQ/7, RZQ/6 (RZQ = 240 Ω)
- Refresh : auto-refresh, self-refresh
- Refresh cycles :
  - Average refresh period
    Commercial: 7.8 µs at 0°C ≤ Tc ≤ +85°C
    3.9 µs at +85°C < Tc ≤ +95°C
    Industrial: 7.8 µs at -40°C ≤ Tc ≤ +85°C
    3.9 µs at +85°C < Tc ≤ +95°
- Operating case temperature range
  Commercial Temperature product 0 °C ≤ Tcase ≤ 95°C
  Industrial Temperature product -40°C ≤ Tcase ≤ 95°C

Option — *Marking*

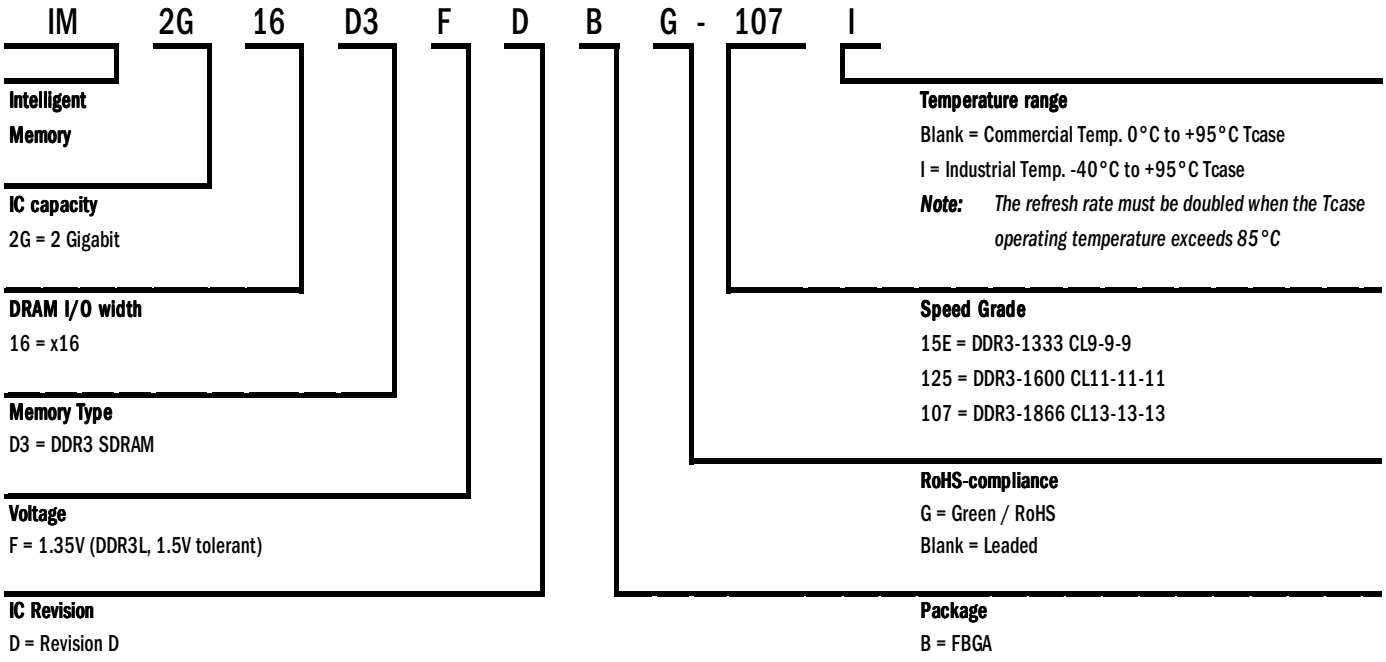
- Configuration
  - 128Mx16 (8 Bank x16Mbit x16) — 2G16
- Package
  - 96-ball FBGA (7.5mm x13mm) for x16 — B
- Leaded/Lead-free
  - Leaded — <blank>
  - Lead-free/RoHS — G
- Speed/Cycle Time
  - 1.07ns @ CL13 (DDR3-1866) — -107
  - 1.25ns @ CL11 (DDR3-1600) — -125
  - 1.5ns @ CL9 (DDR3-1333) — -15E
- Temperature
  - Commercial 0°C to 95°C Tc — <blank>
  - Industrial -40°C to 95°C Tc — I

Example Part Number: IM2G16D3FDBG-107I

Features

- Double-data-rate architecture; two data transfers per clock cycle
- The high-speed data transfer is realized by the 8 bits prefetch pipe-lined architecture
- Bi-directional differential data strobe (DQS and $\overline{\text{DQS}}$) is transmitted/ received with data for capturing data at the receiver
- DQS is edge-aligned with data for READs; center-aligned with data for WRITEs
- Differential clock inputs (CK and $\overline{\text{CK}}$)
- DLL aligns DQ and DQS transitions with CK transitions
- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS
- Data mask (DM) for write data
- Posted $\overline{\text{CAS}}$ by programmable additive latency for better command and data bus efficiency
- On-Die Termination (ODT) for better signal quality
  - Synchronous ODT
  - Dynamic ODT
  - Asynchronous ODT
- Multi Purpose Register (MPR) for pre-defined pattern read out
- ZQ calibration for DQ drive and ODT
- Programmable Partial Array Self-Refresh (PASR)
- $\overline{\text{RESET}}$ pin for Power-up sequence and reset function
- SRT range : Normal/extended
- Programmable Output driver impedance control

Part Number Information



2Gb DDR3 SDRAM Addressing

Configuration	**128Mb x 16**
# of Bank	8
Bank Address	BA0 ~ BA2
Auto precharge	A10/AP
Row Address	A0 ~ A13
Column Address	A0 ~ A9
BC switch on the fly	A12/$\overline{BC}$
Page size	2 KB

Pin Configurations

96-ball FBGA (x16 configuration)

	1	2	3	4	5	6	7	8	9	
A	V_{DDQ}	DQU5	DQU7				DQU4	V_{DDQ}	V_{SS}	A
B	V_{SSQ}	V_{DD}	V_{SS}				$\overline{DQSU}$	DQU6	V_{SSQ}	B
C	V_{DDQ}	DQU3	DQU1				DQSU	DQU2	V_{DDQ}	C
D	V_{SSQ}	V_{DDQ}	DMU				DQU0	V_{SSQ}	V_{DD}	D
E	V_{SS}	V_{SSQ}	DQL0				DML	V_{SSQ}	V_{DDQ}	E
F	V_{DDQ}	DQL2	DQSL				DQL1	DQL3	V_{SSQ}	F
G	V_{SSQ}	DQL6	$\overline{DQSL}$				V_{DD}	V_{SS}	V_{SSQ}	G
H	V_{REFDQ}	V_{DDQ}	DQL4				DQL7	DQL5	V_{DDQ}	H
J	NC	V_{SS}	$\overline{RAS}$				CK	V_{SS}	NC	J
K	ODT	V_{DD}	$\overline{CAS}$				$\overline{CK}$	V_{DD}	CKE	K
L	NC	$\overline{CS}$	$\overline{WE}$				A10/AP	ZQ	NC	L
M	V_{SS}	BA0	BA2				NC	V_{REFCA}	V_{SS}	M
N	V_{DD}	A3	A0				A12/$\overline{BC}$	BA1	V_{DD}	N
P	V_{SS}	A5	A2				A1	A4	V_{SS}	P
R	V_{DD}	A7	A9				A11	A6	V_{DD}	R
T	V_{SS}	$\overline{RESET}$	A13				NC	A8	V_{SS}	T

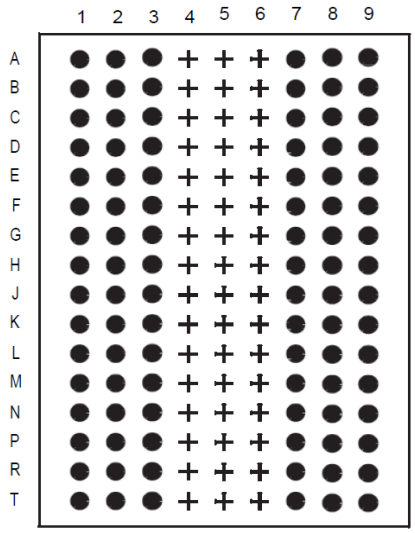
Ball Locations (x16)

● Populated ball

\+ Ball not populated

Top view

(See the balls through the package)

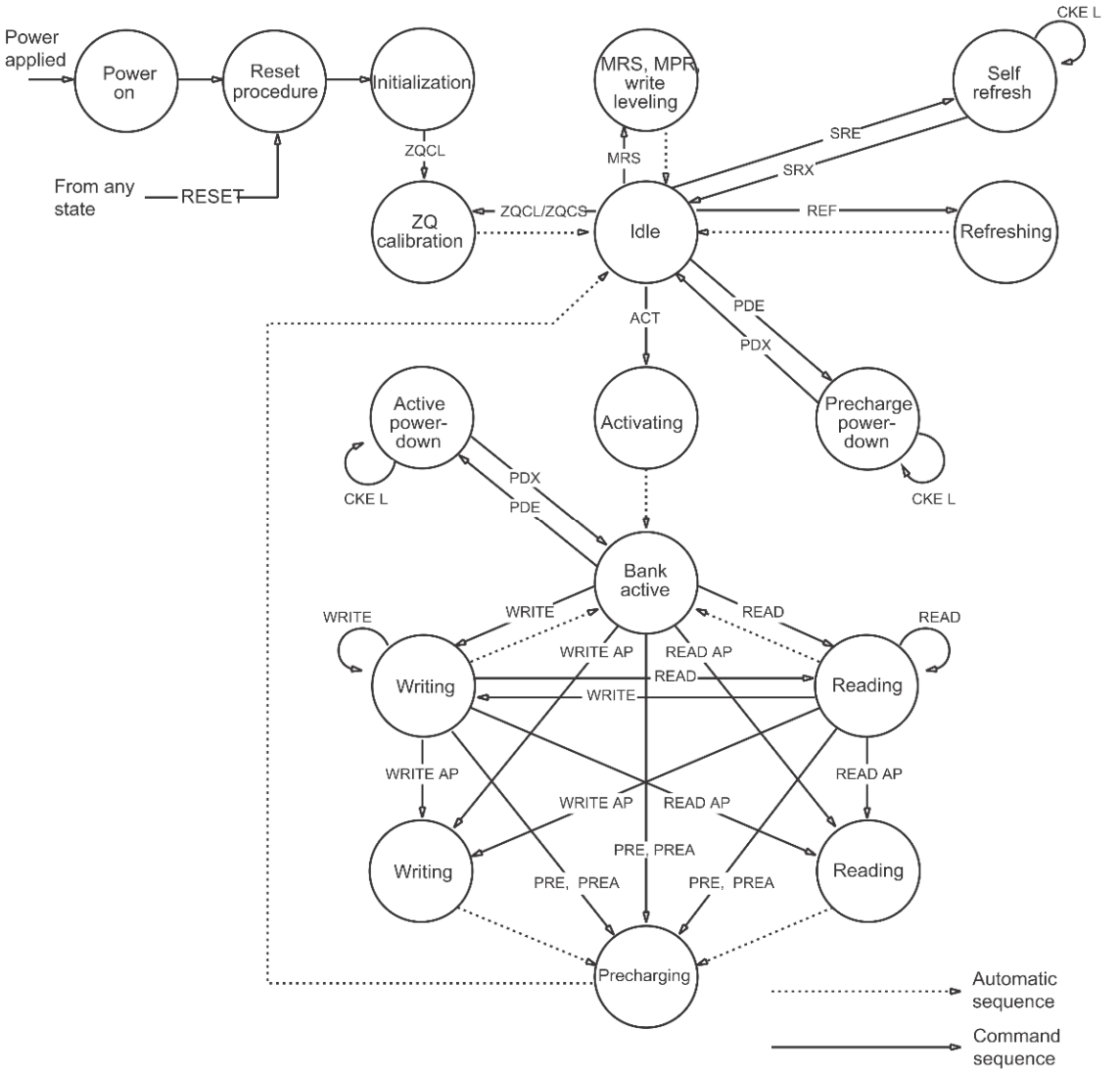


Signal Pin Description

Pin	Type	Function
CK, $\overline{CK}$	Input	**Clock :** CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$. Output (read) data is referenced to the crossings of CK and $\overline{CK}$
CKE	Input	**Clock Enable :** CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self Refresh oper-ation (all banks idle), or Active Power-Down (Row Active in any bank). CKE is asynchronous for self refresh exit. After V_{REFCA} has become stable during the power on and initialization sequence, it must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, $\overline{CK}$, ODT and CKE are disabled during power- down. Input buffers, excluding CKE, are disabled during Self -Refresh.
$\overline{CS}$	Input	**Chip Select :** All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external Rank selection on systems with multiple Ranks. $\overline{CS}$ is considered part of the command code.
ODT	Input	**On Die Termination :** ODT (registered HIGH) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is only applied to each DQ, DQS, $\overline{DQS}$. The ODT pin will be ignored if the Mode Register (MR1) is programmed to disable ODT.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	**Command Inputs :** $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
DMU, DML	Input	**Input Data Mask :** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS.
BA0 - BA2	Input	**Bank Address Inputs :** BA0 - BA2 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 - A13	Input	**Address Inputs :** Provided the row address for Active commands and the column address for Read / Write commands to select one location out of the memory array in the respective bank. (A10/AP and A12/$\overline{BC}$ have additional functions, see below) The address inputs also provide the op-code during Mode Register Set commands.
A10 / AP	Input	**Autoprecharge :** A10 is sampled during Read/Write commands to determine whether Autoprecharge should be per-formed to the accessed bank after the Read/Write operation. (HIGH:Autoprecharge; LOW: No Autoprecharge)A10 is sampled during a Precharge command to determine whether the Pre- charge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / $\overline{BC}$	Input	**Burst Chop :** A12 is sampled during Read and Write commands to determine if burst chop(on-the-fly) will be per-formed. (HIGH : no burst chop, LOW : burst chopped). See command truth table for details.
$\overline{RESET}$	Input	**Active Low Asynchronous Reset :** Reset is active when $\overline{RESET}$ is LOW, and inactive when $\overline{RESET}$ is HIGH. $\overline{RESET}$ must be HIGH during normal operation. $\overline{RESET}$ is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDD, i.e. 1.20V for DC high and 0.30V for DC low.
DQU, DQL, DQSU, $\overline{DQSU}$, DQSL, $\overline{DQSL}$	Input/ Output	**Data Strobe :** Output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobe DQSL and DQSU are paired with differential signals $\overline{DQSL}$ and $\overline{DQSU}$, respectively, to provide differential pair signaling to the system during reads and writes. DDR3 SDRAM supports differential data strobe only and does not support single-ended.

Pin	Type	Function
NC		No Connect: No internal electrical connection is present.
VDDQ	Supply	DQ power supply: 1.35V, 1.283 - 1.45V operational; compatible to 1.5+/- 0.075V operation
VSSQ	Supply	DQ Ground
VDD	Supply	Power Supply: 1.35V, 1.283 - 1.45V operational; compatible to 1.5+/- 0.075V operation.
VSS	Supply	Ground
VREFDQ	Supply	Reference Voltage for DQ
VREFCA	Supply	Reference Voltage for CA
ZQ	Supply	Reference Pin for ZQ calibration
NOTE : Input only pins (BA0-BA2, A0-A13, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$, CKE, ODT and $\overline{RESET}$) do not supply termination.		

Simplified State Diagram



ACT = ACTIVATE
MPR = Multipurpose register
MRS = Mode register set
PDE = Power-down entry
PDX = Power-down exit
PRE = PRECHARGE

PREA = PRECHARGE ALL
READ = RD, RDS4, RDS8
READ AP = RDAP, RDAPS4, RDAPS8
REF = REFRESH
RESET = START RESET PROCEDURE
SRE = Self refresh entry

SRX = Self refresh exit
WRITE = WR, WRS4, WRS8
WRITE AP = WRAP, WRAPS4, WRAPS8
ZQCL = ZQ LONG CALIBRATION
ZQCS = ZQ SHORT CALIBRATION

Basic Functionality

Read and write operation to the DDR3 SDRAM are burst oriented, start at a selected location, and continue for a burst length of four or eight in a programmed sequence. Operation begins with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the Active command are used to select the bank and row to be accessed (BA0-BA2 select the bank; A0-A13 select the row).The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst operation, determine if the auto precharge command is to be issued (via A10/AP), and the select BC4 or BL8 mode “on the fly” (via A12) if enabled in the mode register.

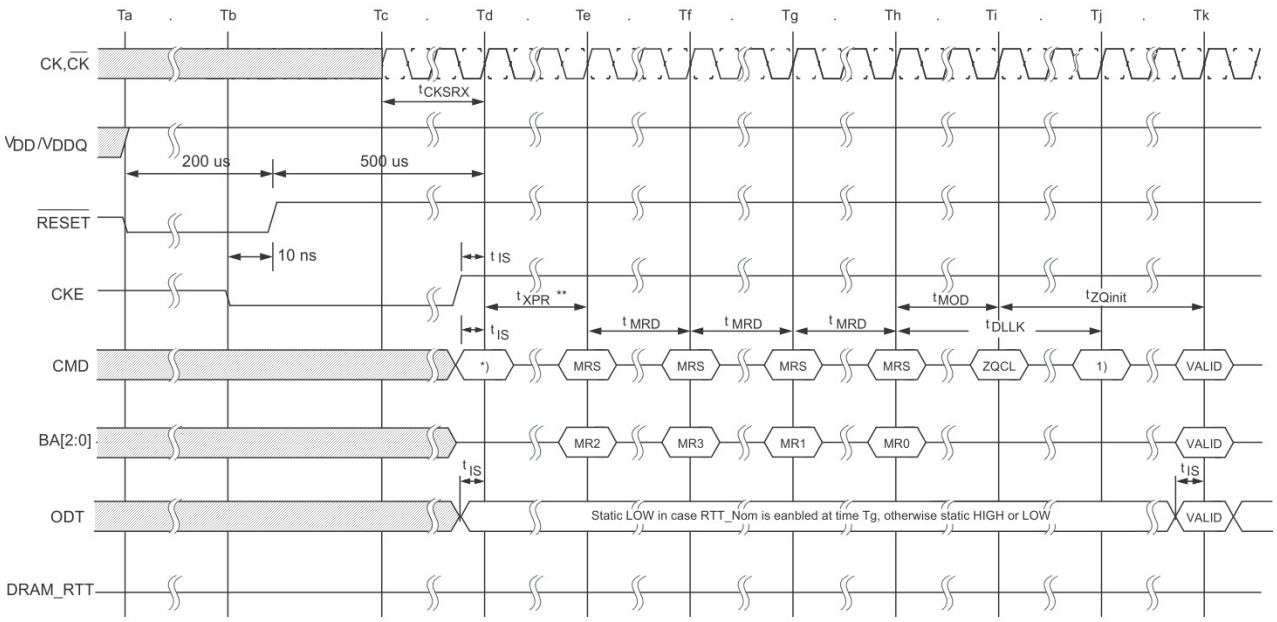
Prior to normal operation, the DDR3 SDRAM must be powered up and initialized in a predefined manner. The following sections provide detailed information covering device reset and initialization, register definition, command descriptions and device operation.

Power-up and Initialization Sequence

The following sequence is required for POWER UP and Initialization.

1. Apply power and attempt to maintain $\overline{\text{RESET}}$ below 0.2 x VDD (all other inputs may be undefined). $\overline{\text{RESET}}$ needs to be maintained for minimum 200µs with stable power. CKE is pulled “Low” anytime before $\overline{\text{RESET}}$ being de-asserted (min time 10ns). The power voltage ramp time between 300mV to VDD min must be no longer than 200ms; and during the ramp, VDD > VDDQ and VDD -VDDQ < 0.3 volts.
   - VDD and VDDQ are driven from a single power converter output, AND
   - The voltage levels on all pins other than VDD,VDDQ,VSS,VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side. In addition, VTT is limited to 0.95V max once power ramp is finished, AND
   - VREF tracks VDDQ/2.

   or
   - Apply VDD without any slope reversal before or at the same time as VDDQ.
   - Apply VDDQ without any slope reversal before or at the same time as VTT & VREF.
   - The voltage levels on all pins other than VDD,VDDQ,VSS,VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side.
2. After $\overline{\text{RESET}}$ is de-asserted, wait for another 500us until CKE becomes active. During this time, the DRAM will start internal initialization; this will be done independently of external clocks.
3. Clocks (CK, $\overline{\text{CK}}$) need to be started and stabilized for at least 10ns or 5tCK (which is larger) before CKE goes active. Since CKE is a synchronous signal, the corresponding setup time to clock (tIS) must be met. Also a NOP or Deselect command must be registered (with tIS set up time to clock) before CKE goes active. Once the CKE registered “High” after Reset, CKE needs to be continuously registered “High” until the initialization sequences finished, including expiration of tDLLK and tZQinit.
4. The DDR3 SDRAM keeps its on-die termination in high-impedance state as long as $\overline{\text{RESET}}$ is asserted. Further, the SDRAM keeps its on-die termination in high impedance state after $\overline{\text{RESET}}$ deassertion until CKE is registered HIGH. The ODT input signal may be in undefined state until tIS before CKE is registered HIGH. When CKE is registered HIGH, the ODT input signal may be statically held at either LOW or HIGH. If RTT_NOM is to be enabled in MR1 and the on-die termination is required to remain in the high impedance state, the ODT input signal must be statically held LOW. In all cases, the ODT input signal remains static until the power up initialization sequence is finished, including the expiration of tDLLK and tZQinit.
5. After CKE is registered high, wait minimum of Reset CKE Exit time, tXPR, before issuing the first MRS command to load mode register.(tXPR=Max(tXS, 5tCK)]
6. Issue MRS Command to load MR2 with all application settings. (To issue MRS command for MR2, provide “Low” to BA0 and BA2, “High” to BA1.)
7. Issue MRS Command to load MR3 with all application settings. (To issue MRS command for MR3, provide “Low” to BA2, “High” to BA0 and BA1.)
8. Issue MRS Command to load MR1 with all application settings and DLL enabled. (To issue ”DLL Enable” command, provide “Low” to A0, ”High” to BA0 and “Low” to BA1-BA2)
9. Issue MRS Command to load MR0 with all application settings and “DLL reset”. (To issue DLL reset command, provide “High” to A8 and “Low” to BA0-2).
10. Issue ZQCL command to starting ZQ calibration.
11. Wait for both tDLLK and tZQ init completed.
12. The DDR3 SDRAM is now ready for normal operation.

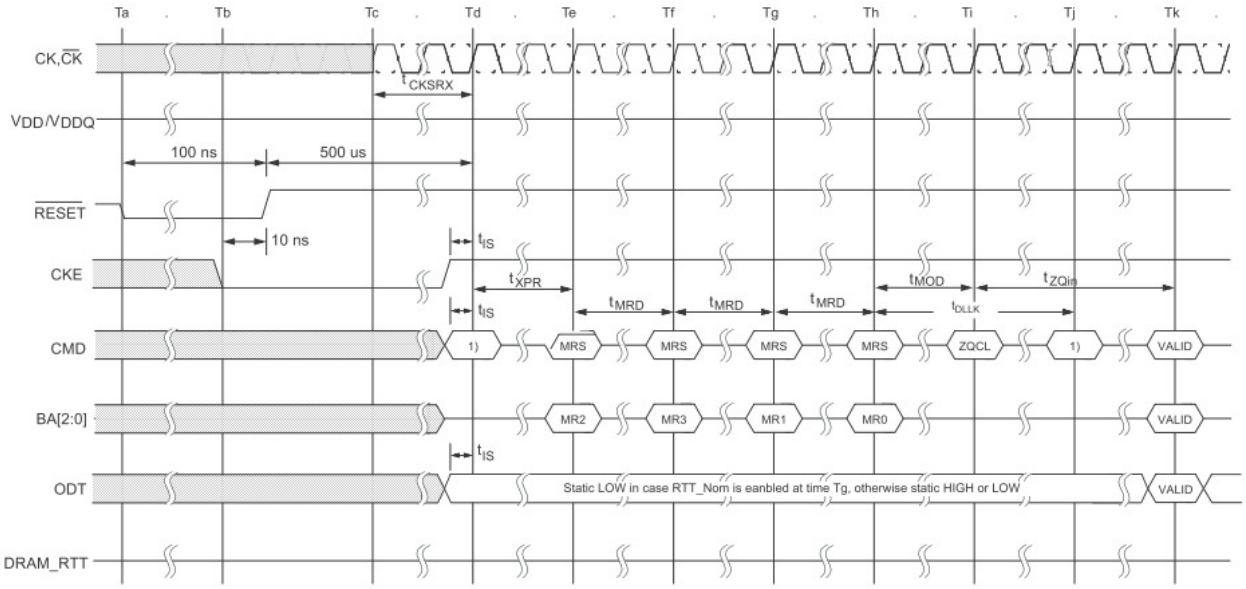


1) From time point 'Td' until 'Tk', NOP or DES commands must be applied between MRS and ZQCL commands

Reset and Initialization with Stable Power

The following sequence is required for /RESET at no power interruption initialization.

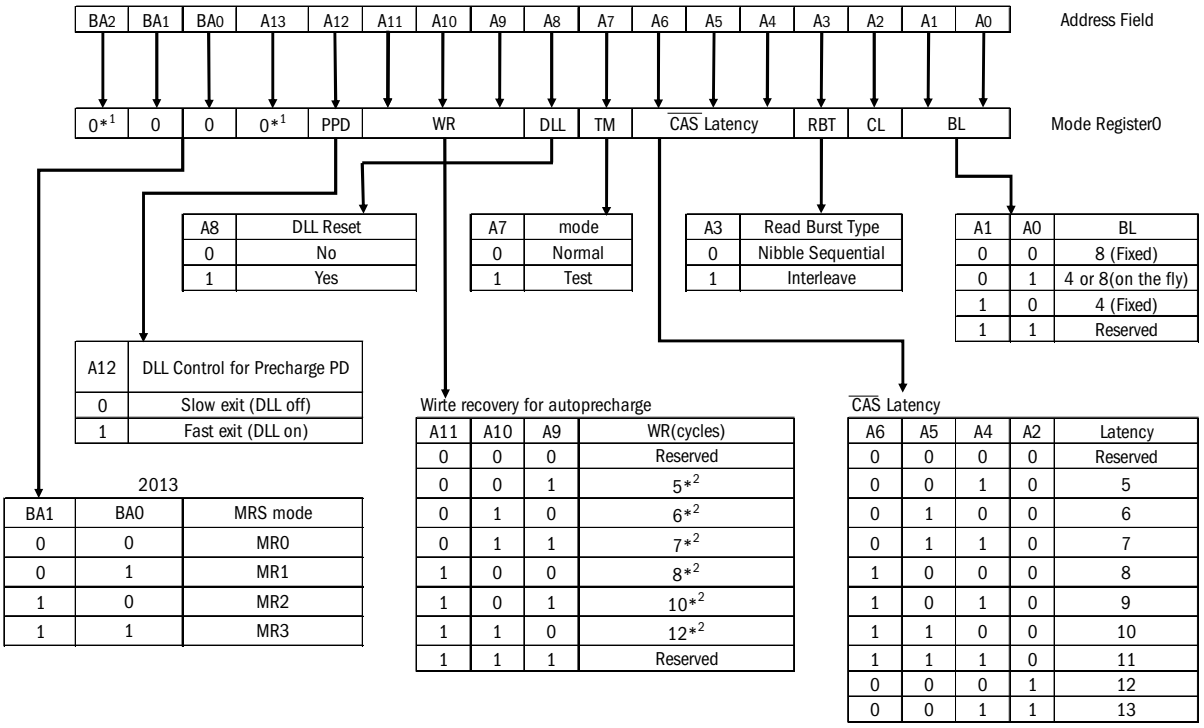
1. Assert /RESET below 0.2 x VDD anytime when reset is needed (all other inputs may be undefined). /RESET needs to be maintained for minimum 100ns. CKE is pulled low before /RESET being de-asserted (minimum time 10ns).
2. Follow Power-Up Initialization Sequence steps 2 to 11.
3. The reset sequence is now completed; DDR3 SDRAM is ready for normal operation.



1) From time point 'Td' until 'Tk', NOP or DES commands must be applied between MRS and ZQCL commands

Mode Register MR0

The Mode Register MR0 stores the data for controlling various operating modes of DDR3 SDRAM. It controls burst length, read burst type, $\overline{CAS}$ latency, test mode, DLL reset, WR and DLL control for precharge power-down, which include various vendor specific options to make DDR3 SDRAM useful for various applications. The mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, BA0, BA1 and BA2, while controlling the states of address pins according to the table below.



A8	DLL Reset
0	No
1	Yes

A7	mode
0	Normal
1	Test

A3	Read Burst Type
0	Nibble Sequential
1	Interleave

A1	A0	BL
0	0	8 (Fixed)
0	1	4 or 8(on the fly)
1	0	4 (Fixed)
1	1	Reserved

A12	DLL Control for Precharge PD
0	Slow exit (DLL off)
1	Fast exit (DLL on)

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BA1	BA0	MRS mode
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

Write recovery for autoprecharge

A11	A10	A9	WR(cycles)
0	0	0	Reserved
0	0	1	5*2
0	1	0	6*2
0	1	1	7*2
1	0	0	8*2
1	0	1	10*2
1	1	0	12*2
1	1	1	Reserved

$\overline{CAS}$ Latency

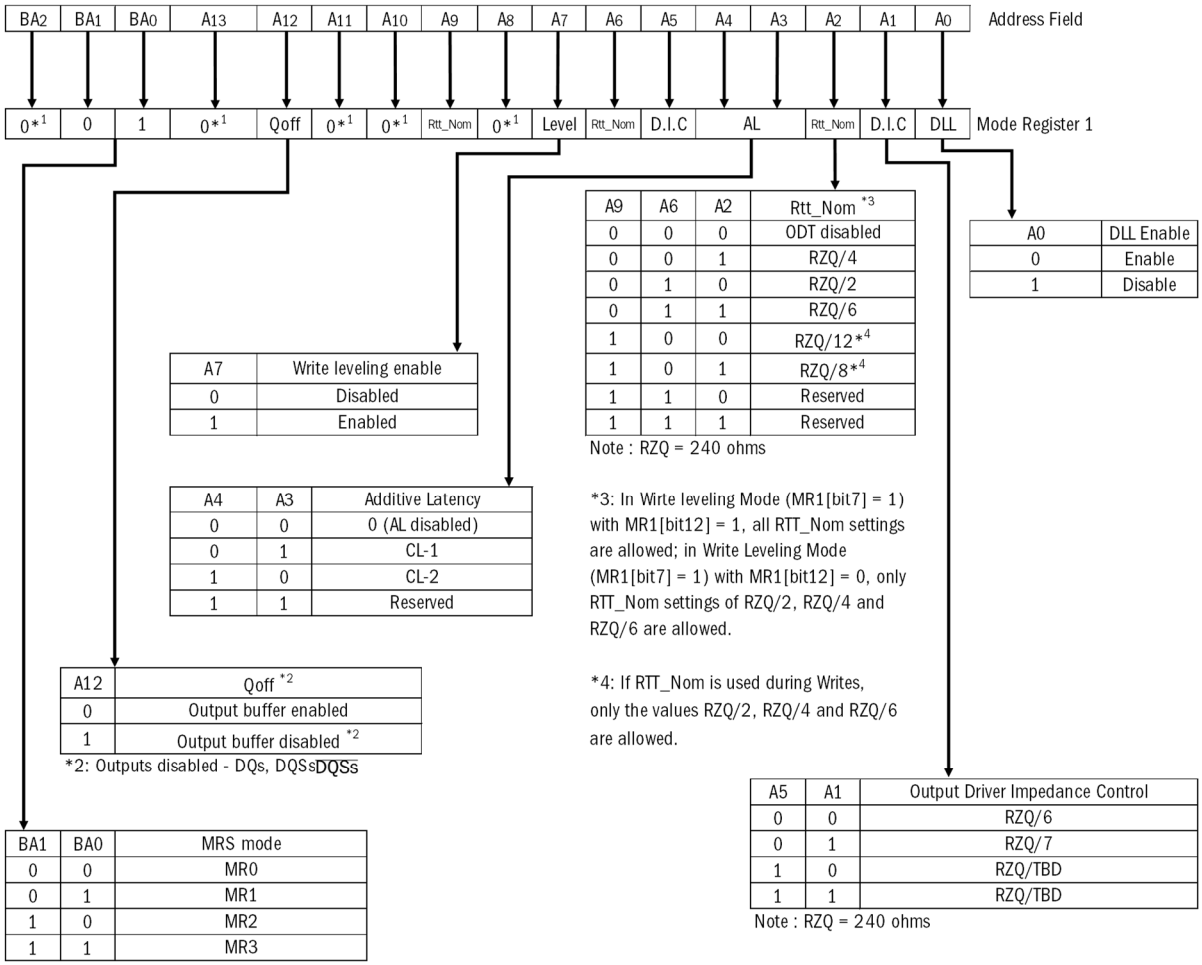
A6	A5	A4	A2	Latency
0	0	0	0	Reserved
0	0	1	0	5
0	1	0	0	6
0	1	1	0	7
1	0	0	0	8
1	0	1	0	9
1	1	0	0	10
1	1	1	0	11
0	0	0	1	12
0	0	1	1	13

*1 : BA2 and A13 are reserved for future use and must be programmed to 0 during MRS.

*2 : WR(write recovery for autoprecharge)min in clock cycles is calculated by dividing tWR(in ns) by tCK(in ns) and rounding up to the next integer: WRmin[cycles] = Roundup(tWR[ns]/tCK[ns]). The WR value in the mode register must be programmed to be equal or larger than WRmin The programmed WR value is used with tRP to determine tDAL.

Mode Register MR1

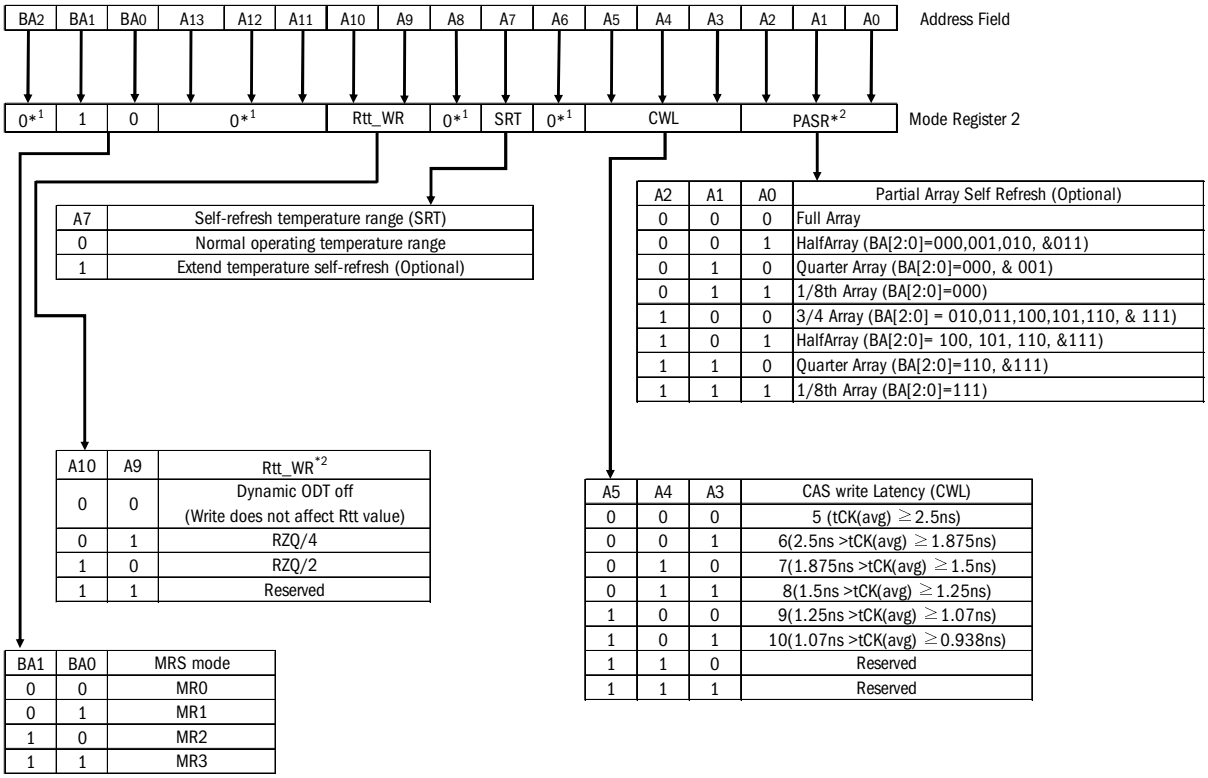
The Mode Register MR1 stores the data for enabling or disabling the DLL, output driver strength, RTT_Nom impedance, additive latency, write leveling enable and Qoff.
The Mode Register 1 is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, high on BA0, low on BA1 and BA2, while controlling the states of address pins according to the table below.



*1 : BA2, A8, A10, A11 and A13 are reserved for future use (RFU) and must be programmed to 0 during MRS.

Mode Register MR2

The Mode Register MR2 stores the data for controlling refresh related features, RTT_WR impedance and CAS write latency (CWL). The Mode Register 2 is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, high on BA1, low on BA0 and BA2, while controlling the states of address pins according to the table below.



A7	Self-refresh temperature range (SRT)
0	Normal operating temperature range
1	Extend temperature self-refresh (Optional)

A2	A1	A0	Partial Array Self Refresh (Optional)
0	0	0	Full Array
0	0	1	HalfArray (BA[2:0]=000,001,010, &011)
0	1	0	Quarter Array (BA[2:0]=000, & 001)
0	1	1	1/8th Array (BA[2:0]=000)
1	0	0	3/4 Array (BA[2:0] = 010,011,100,101,110, & 111)
1	0	1	HalfArray (BA[2:0]= 100, 101, 110, &111)
1	1	0	Quarter Array (BA[2:0]=110, &111)
1	1	1	1/8th Array (BA[2:0]=111)

A10	A9	Rtt_WR*2
0	0	Dynamic ODT off (Write does not affect Rtt value)
0	1	RZQ/4
1	0	RZQ/2
1	1	Reserved

A5	A4	A3	CAS write Latency (CWL)
0	0	0	5 (tCK(avg) ≥ 2.5ns)
0	0	1	6(2.5ns >tCK(avg) ≥ 1.875ns)
0	1	0	7(1.875ns >tCK(avg) ≥ 1.5ns)
0	1	1	8(1.5ns >tCK(avg) ≥ 1.25ns)
1	0	0	9(1.25ns >tCK(avg) ≥ 1.07ns)
1	0	1	10(1.07ns >tCK(avg) ≥ 0.938ns)
1	1	0	Reserved
1	1	1	Reserved

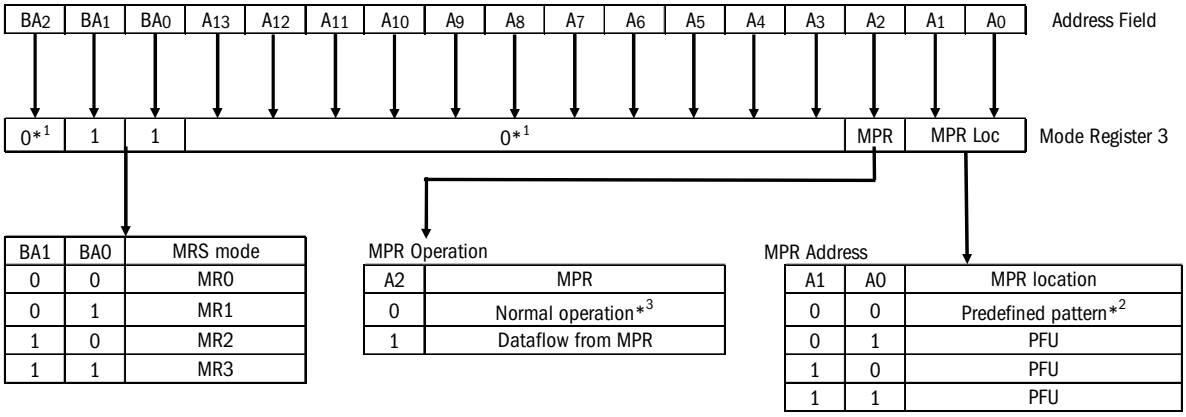
BA1	BA0	MRS mode
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

*1 : BA2, A8, A11 ~ A13 are RFU and must be programmed to 0 during MRS.

*2 : The Rtt_WR value can be applied during writes even when Rtt_Nom is disabled. During write leveling, Dynamic ODT is not available.

Mode Register MR3

The Mode Register MR3 controls Multi Purpose Registers (MPR). The Mode Register 3 is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, high on BA1 and BA0, and low on BA2 while controlling the states of address pins according to the table below.



BA1	BA0	MRS mode
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

MPR Operation

A2	MPR
0	Normal operation*3
1	Dataflow from MPR

MPR Address

A1	A0	MPR location
0	0	Predefined pattern*2
0	1	PFU
1	0	PFU
1	1	PFU

*1 : BA2, A3 - A13 are reserved for future use (RFU) and must be programmed to 0 during MRS.
*2 : The predefined pattern will be used for read synchronization.
*3 : When MPR control is set for normal operation, MP3 A[2] = 0, MR3 A[1:0] will be ignored.

Burst Length (MR0)

Read and write accesses to the DDR3 are burst oriented, with the burst length being programmable, as shown in the figure MR0 Programming. The burst length determines the maximum number of column locations that can be accessed for a given read or write command. Burst length options include fixed BC4, fixed BL8, and on the fly which allows BC4 or BL8 to be selected coincident with the registration of a read on write command Via A12 ($\overline{BC}$). Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

Burst Chop

In case of burst length being fixed to 4 by MR0 setting, the internal write operation starts two clock cycles earlier than for the BL8 mode. This means that the starting point for tWR and tWTR will be pulled in by two clocks. In case of burst length being selected on the fly via A12($\overline{BC}$), the internal write operation starts at the same point in time like a burst of 8 write operation. This means that during on-the-fly control, the starting point for tWR and tWTR will not be pulled in by two clocks.

Burst Type (MR0)

[Burst Length and Sequence]

Burst length	Operation	Starting address (A2, A1, A0)	Sequential addressing (decimal)	Interleave addressing (decimal)
4 (Burst chop)	READ	000	0, 1, 2, 3, T, T, T, T	0, 1, 2, 3, T, T, T, T
		001	1, 2, 3, 0, T, T, T, T	1, 0, 3, 2, T, T, T, T
		010	2, 3, 0, 1, T, T, T, T	2, 3, 0, 1, T, T, T, T
		011	3, 0, 1, 2, T, T, T, T	3, 2, 1, 0, T, T, T, T
		100	4, 5, 6, 7, T, T, T, T	4, 5, 6, 7, T, T, T, T
		101	5, 6, 7, 4, T, T, T, T	5, 4, 7, 6, T, T, T, T
		110	6, 7, 4, 5, T, T, T, T	6, 7, 4, 5, T, T, T, T
		111	7, 4, 5, 6, T, T, T, T	7, 6, 5, 4, T, T, T, T
	WRITE	0VV	0, 1, 2, 3, X, X, X, X	0, 1, 2, 3, X, X, X, X
		1VV	4, 5, 6, 7, X, X, X, X	4, 5, 6, 7, X, X, X, X
8	READ	000	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
		001	1, 2, 3, 0, 5, 6, 7, 4	1, 0, 3, 2, 5, 4, 7, 6
		010	2, 3, 0, 1, 6, 7, 4, 5	2, 3, 0, 1, 6, 7, 4, 5
		011	3, 0, 1, 2, 7, 4, 5, 6	3, 2, 1, 0, 7, 6, 5, 4
		100	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
		101	5, 6, 7, 4, 1, 2, 3, 0	5, 4, 7, 6, 1, 0, 3, 2
		110	6, 7, 4, 5, 2, 3, 0, 1	6, 7, 4, 5, 2, 3, 0, 1
		111	7, 4, 5, 6, 3, 0, 1, 2	7, 6, 5, 4, 3, 2, 1, 0
	WRITE	VVV	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7

Remark: T: Output driver for data and strobes are in high impedance.

V: A valid logic level (0 or 1), but respective buffer input ignores level on input pins. X: Don't Care.

Notes: 1. Page length is a function of I/O organization and column addressing

2. 0...7 bit number is value of CA [2:0] that causes this bit to be the first read during a burst.

Command Truth Table

(a) Note 1,2,3,4 apply to the entire Command truth table
(b) Note 5 applies to all Read/Write commands.
[BA=Bank Address, RA=Row Address, CA=Column Address, $\overline{BC}$=Burst Chop, X=Don't care, V=Valid]

Function	Abbreviation	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0 - BA2	A13	A12 / $\overline{BC}$	A10 / AP	A0 - A9,A11	Notes
		Previous Cycle	Current Cycle										
Mode Register Set	MRS	H	H	L	L	L	L	BA	OP Code				
Refresh	REF	H	H	L	L	L	H	V	V	V	V	V	
Self Refresh Entry	SRE	H	L	L	L	L	H	V	V	V	V	V	7,9,12
Self Refresh Exit	SRX	L	H	H	X	X	X	X	X	X	X	X	7,8,9,12
				L	H	H	H	V	V	V	V	V	
Single Bank Precharge	PRE	H	H	L	L	H	L	BA	V	V	L	V	
Precharge all Banks	PREA	H	H	L	L	H	L	V	V	V	H	V	
Bank Activate	ACT	H	H	L	L	H	H	BA	Row Address (RA)				
Write (Fixed BL8 or BL4)	WR	H	H	L	H	L	L	BA	RFU	V	L	CA	
Write (BL4, on the Fly)	WRS4	H	H	L	H	L	L	BA	RFU	L	L	CA	
Write (BL8, on the Fly)	WRS8	H	H	L	H	L	L	BA	RFU	H	L	CA	
Write with Auto Precharge (Fixed BL8 or BL4)	WRA	H	H	L	H	L	L	BA	RFU	V	H	CA	
Write with Auto Precharge (BL4, on the Fly)	WRAS4	H	H	L	H	L	L	BA	RFU	L	H	CA	
Write with Auto Precharge (BL8, on the Fly)	WRAS8	H	H	L	H	L	L	BA	RFU	H	H	CA	
Read (Fixed BL8 or BL4)	RD	H	H	L	H	L	H	BA	RFU	V	L	CA	
Read (BL4, on the Fly)	RDS4	H	H	L	H	L	H	BA	RFU	L	L	CA	
Read (BL8, on the Fly)	RDS8	H	H	L	H	L	H	BA	RFU	H	L	CA	
Read with Auto Precharge (Fixed BL8 or BL4)	RDA	H	H	L	H	L	H	BA	RFU	V	H	CA	
Read with Auto Precharge (BL4, on the Fly)	RDAS4	H	H	L	H	L	H	BA	RFU	L	H	CA	
Read with Auto Precharge (BL8, on the Fly)	RDAS8	H	H	L	H	L	H	BA	RFU	H	H	CA	
No Operation	NOP	H	H	L	H	H	H	V	V	V	V	V	10
Device Deselected	DES	H	H	H	X	X	X	X	X	X	X	X	11
ZQ calibration Long	ZQCL	H	H	L	H	H	L	X	X	X	H	X	
ZQ calibration Short	ZQCS	H	H	L	H	H	L	X	X	X	L	X	
Power Down Entry	PDE	H	L	L	H	H	H	V	V	V	V	V	6,12
				H	X	X	X	X	X	X	X	X	
Power Down Exit	PDX	L	H	L	H	H	H	V	V	V	V	V	6,12
				H	X	X	X	X	X	X	X	X	

Note :

1. All DDR3 SDRAM commands are defined by states of $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and CKE at the rising edge of the clock. The MSB of BA, RA, and CA are device density and configuration dependant
2. $\overline{RESET}$ is Low enable command which will be used only for asynchronous reset so must be maintained HIGH during any function.
3. Bank addresses (BA) determine which bank is to be operated upon. For (E)MRS BA selects an (Extended) Mode Register
4. "V" means "H or L (but a defined logic level)" and "X" means either "defined or undefined (like floating) logic level"
5. Burst reads or writes cannot be terminated or interrupted and Fixed/on the fly BL will be defined by MRS
6. The Power Down Mode does not perform any refresh operations.
7. The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.
8. Self refresh exit is asynchronous.
9. V_{REF}(Both V_{REFDQ} and V_{REFCA}) must be maintained during Self Refresh operation.
10. The No Operation command (NOP) should be used in cases when the DDR3 SDRAM is in an idle or a wait state. The purpose of the No Operation command (NOP) is to prevent the DDR3 SDRAM from registering any unwanted commands between operations. A No Operation command will not terminate a previous operation that is still executing, such as a burst read or write cycle.
11. The Deselect command performs the same function as a No Operation command.
12. Refer to the CKE Truth Table for more detail with CKE transition

CKE Truth Table

(a) Note 1~7 apply to the entire Command truth table
(b) CKE low is allowed only if tMRD and tMOD are satisfied

Current State [2]	CKE		Command (N) [3] $\overline{RAS}, \overline{CAS}, \overline{WE}, \overline{CS}$	Action (N)[3]	Notes
	Previous Cycle [1] (N-1)	Current Cycle [1] (N)			
Power Down	L	L	X	Maintain Power-Down	14, 15
	L	H	DESELECT or NOP	Power Down Exit	11, 14
Self Refresh	L	L	X	Maintain Self Refresh	15, 16
	L	H	DESELECT or NOP	Self Refresh Exit	8, 12, 16
Bank(s) Active	H	L	DESELECT or NOP	Active Power Down Entry	11, 13, 14
Reading	H	L	DESELECT or NOP	Power Down Entry	11, 13, 14, 17
Writing	H	L	DESELECT or NOP	Power Down Entry	11, 13, 14, 17
Precharging	H	L	DESELECT or NOP	Power Down Entry	11, 13, 14, 17
Refreshing	H	L	DESELECT or NOP	Precharge Power Down Entry	11
All Banks Idle	H	L	DESELECT or NOP	Precharge Power Down Entry	11,13, 14, 18
	H	L	REFRESH	Self Refresh Entry	9, 13, 18
For more details with all signals See "Command Truth Table," on previous page					10

Notes:
1. CKE (N) is the logic state of CKE at clock edge N; CKE (N–1) was the state of CKE at the previous clock edge.
2. Current state is defined as the state of the DDR3 SDRAM immediately prior to clock edge N
3. COMMAND (N) is the command registered at clock edge N, and ACTION (N) is a result of COMMAND (N), ODT is not included here
4. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document
5. The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh
6. CKE must be registered with the same value on tCKEmin consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the tCKEmin clocks of registeration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of tIS + tCKEmin + tIH.
7. DESELECT and NOP are defined in the Command truth table
8. On Self Refresh Exit DESELECT or NOP commands must be issued on every clock edge occurring during the tXS period. Read or ODT commands may be issued only after tXSDLL is satisfied.
9. Self Refresh mode can only be entered from the All Banks Idle state.
10. Must be a legal command as defined in the Command Truth Table.
11. Valid commands for Power Down Entry and Exit are NOP and DESELECT only.
12. Valid commands for Self Refresh Exit are NOP and DESELECT only.
13. Self Refresh can not be entered while Read or Write operations. See 'Self-Refresh Operation" and 'Power-Down Modes" on later section for a detailed list of restrictions.
14. The Power Down does not perform any refresh operations.
15. "X" means "don't care (including floating around V_{REF})" in Self Refresh and Power Down. It also applies to Address pins
16. V_{REF} (Both V_{REFDQ} and V_{REFCA}) must be maintained during Self Refresh operation.
17. If all banks are closed at the conclusion of the read, write or precharge command, then Precharge Power Down is entered, otherwise Active Power Down is entered
18. 'Idle state' means that all banks are closed(tRP,tDAL,etc. satisfied) and CKE is high and all timings from previous operations are satisfied (tMRD,tMOD,tRFC,tZQinit,tZQoper,tZQCS,etc)as well as all SRF exit and Power Down exit parameters are satisfied (tXS,tXP,tXPDLL,etc)

Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	Notes
VDD	Voltage on VDD pin relative to VSS	-0.4 ~ 1.8	V	1,3
VDDQ	Voltage on VDDQ pin relative to VSS	-0.4 ~ 1.8	V	1,3
VIN, VOUT	Voltage on any pin relative to VSS	-0.4 ~ 1.8	V	1
TSTG	Storage Temperature	-55 to +100	°C	1,2

NOTE :

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indi-cated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. V_{DD} and V_{DDQ} must be within 300mV of each other at all times; and V_{REF} must be not greater than 0.6 x V_{DDQ}, When V_{DD} and V_{DDQ} are less than 500mV; V_{REF} may be equal to or less than 300mV.

Operating Temperature Condition

Symbol	Parameter	Rating		Unit	Notes
		Min	Max		
Tcase	Case operating temperature for commercial temperature product	0	95	°C	1,2,3
Tcase	Case operating temperature for industrial temperature product	-40	95	°C	1,2,3

NOTE :

1. Operating temperature is the case surface temperature on the center/top side of the DRAM.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation this temperature range must be maintained under all operating conditions.
3. Some applications require operation of the DRAM in the Extended Temperature Range between +85°C and +105°C case temperature. Full specifications are guaranteed in this range, but the following additional conditions applies:

   a) Refresh commands must be doubled in frequency, therefore reducing the refresh interval tREFI to 3.9μs. (This double refresh requirement may not apply for some devices.)

   b) If Self-refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 bit [A6, A7] = [0, 1]) or enable the optional Auto Self-Refresh mode (MR2 bit [A6, A7] = [1, 0]).

Recommended DC Operating Conditions

Symbol	Parameter	Operation Voltage	Rating			Units	Notes
			Min	Typ	Max		
VDD	Supply voltage	1.35	1.283	1.35	1.45	V	1,2,3
		1.5	1.425	1.5	1.575	V	1,2,3
VDDQ	Supply voltage for Output	1.35	1.283	1.35	1.45	V	1,2,3
		1.5	1.425	1.5	1.575	V	1,2,3

NOTE :

1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
3. VDD and VDDQ rating are determinated by operation voltage.

AC and DC Input Measurement Levels

Single-Ended AC and DC Input Levels for Command and Address (1.35V)

Symbol	Parameter	Min	Max	Units	Notes
VIHCA (DC90)	DC input logic high	VREF + 0.090	VDD	V	1,5(a)
VILCA (DC90)	DC input logic low	VSS	VREF - 0.090	V	1,6(a)
VIHCA (AC160)	AC input logic high DDR3L-1600, 1333	VREF + 0.160	-	V	1,2
	DDR3L-1866	-	-		
VILCA (AC160)	AC input logic low DDR3L-1600, 1333	-	VREF - 0.160	V	1,2
	DDR3L-1866	-	-		
VIHCA (AC135)	AC input logic high DDR3L-1600, 1333	VREF + 0.135	-	V	1,2
	DDR3L-1866	VREF + 0.135	-		
VILCA (AC135)	AC input logic low DDR3L-1600, 1333	-	VREF - 0.135	V	1,2
	DDR3L-1866	-	VREF - 0.135		
VIHCA (AC125)	AC input logic high DDR3L-1600, 1333	-	-	V	1,2
	DDR3L-1866	VREF + 0.125	-		
VILCA (AC125)	AC input logic low DDR3L-1600, 1333	-	-	V	1,2
	DDR3L-1866	-	VREF - 0.125		
VREFCA (DC)	Reference voltage for ADD, CMD inputs	0.49 * VDD	0.51 * VDD	V	3,4

Single-Ended AC and DC Input Levels for Command and Address (1.5V)

Symbol	Parameter	Min	Max	Units	Notes
VIHCA (DC100)	DC input logic high	VREF + 0.100	VDD	V	1, 5(b)
VILCA (DC100)	DC input logic low	VSS	VREF - 0.100	V	1, 6(b)
VIHCA (AC175)	AC input logic high DDR3-1600, 1333	VREF + 0.175	-	V	1,2,7
	DDR3-1866	-	-		
VILCA (AC175)	AC input logic low DDR3-1600, 1333	-	VREF - 0.175	V	1,2,8
	DDR3-1866	-	-		
VIHCA (AC150)	AC input logic high DDR3-1600, 1333	VREF + 0.150	-	V	1,2,7
	DDR3-1866	-	-		
VILCA (AC150)	AC input logic low DDR3-1600, 1333	-	VREF - 0.150	V	1,2,8
	DDR3-1866	-	-		
VIHCA (AC135)	AC input logic high DDR3-1600, 1333	-	-	V	1,2
	DDR3-1866	VREF + 0.135	-		
VILCA (AC135)	AC input logic low DDR3-1600, 1333	-	-	V	1,2
	DDR3-1866	-	VREF - 0.135		
VIHCA (AC125)	AC input logic high DDR3-1600, 1333	-	-	V	1,2
	DDR3-1866	VREF + 0.125	-		
VILCA (AC125)	AC input logic low DDR3-1600, 1333	-	-	V	1,2
	DDR3-1866	-	VREF - 0.125		
VREFCA (DC)	Reference voltage for ADD, CMD inputs	0.49 * VDD	0.51 * VDD	V	3,4

NOTE :
1. For input only pins except /RESET : VREF = VREFCA (DC).
2. See Overshoot and Undershoot Specifications section.
3. The AC peak noise on VREF may not allow VREF to deviate from VREFCA (DC) by more than ±1% VDD (for reference : approx. ±15 mV).
4. For reference : approx. VDD/2 ±15 mV.
5. VIH(dc) is used as a simplified symbol for VIH.CA(a) 1.35V : DC90, b) 1.5V : DC100)
6. VIL(dc) is used as a simplified symbol for VIL.CA(a) 1.35V : DC90, b) 1.5V : DC100)
7. VIH(ac) is used as a simplified symbol for VIH.CA(AC175) and VIH.CA(AC150); VIH.CA(AC175) value is used when VREF + 175mV is referenced and VIH.CA(AC150) value is used when VREF + 150mV is referenced.
8. VIL(ac) is used as a simplified symbol for VIL.CA(AC175) and VIL.CA(AC150); VIL.CA(AC175) value is used when VREF - 175mV is referenced and VIL.CA(AC150) value is used when VREF - 150mV is referenced.

Single-Ended AC and DC Input Levels for DQ and DM (1.35V)

Symbol	Parameter	Min	Max	Units	Notes
VIHDQ (DC90)	DC input logic high	VREF + 0.090	VDD	V	1,5(a)
VILDQ (DC90)	DC input logic low	VSS	VREF - 0.090	V	1,6(a)
VIHDQ (AC160)	DDR3L-1866, 1600, 1333	-	-	V	1,2
VILDQ (AC160)	AC input logic low DDR3L-1866, 1600, 1333	-	-	V	1,2
VIHDQ (AC135)	AC input logic high DDR3L-1866, 1600, 1333	VREF + 0.135	-	V	1,2
VILDQ (AC135)	AC input logic low DDR3L-1866, 1600, 1333	-	VREF - 0.135	V	1,2
VIHDQ (AC130)	AC input logic high DDR3L-1600, 1333	-	-	V	1,2
	DDR3L-1866	VREF + 0.130	-		
VILDQ (AC130)	AC input logic low DDR3L-1600, 1333	-	-	V	1,2
	DDRL-1866	-	VREF - 0.130		
VREFDQ (DC)	Reference voltage for DQ, DM inputs	0.49 * VDD	0.51 * VDD	V	3,4

Single-Ended AC and DC Input Levels for DQ and DM (1.5V)

Symbol	Parameter	Min	Max	Units	Notes
VIHDQ (DC100)	DC input logic high	VREF + 0.100	VDD	V	1,5(b)
VILDQ (DC100)	DC input logic low	VSS	VREF - 0.100	V	1,6(b)
VIHDQ (AC175)	DDR3-1866, 1600, 1333	-	-	V	1,2,7
VILDQ (AC175)	DDR3-1866, 1600, 1333	-	-	V	1,2,8
VIHDQ (AC150)	AC input logic high DDR3-1600, 1333	VREF + 0.150	-	V	1,2,7
	DDR3-1866	-	-		
VILDQ (AC150)	AC input logic low DDR3-1600, 1333	-	VREF - 0.150	V	1,2,8
	DDR3-1866	-	-		
VIHDQ (AC135)	AC input logic high DDR3-1600, 1333	-	-	V	1,2
	DDR3-1866	VREF + 0.135	-		
VILDQ (AC135)	AC input logic low DDR3-1600, 1333	-	-	V	1,2
	DDR3-1866	-	VREF - 0.135		
VREFDQ (DC)	Reference voltage for DQ, DM inputs	0.49 * VDD	0.51 * VDD	V	3,4

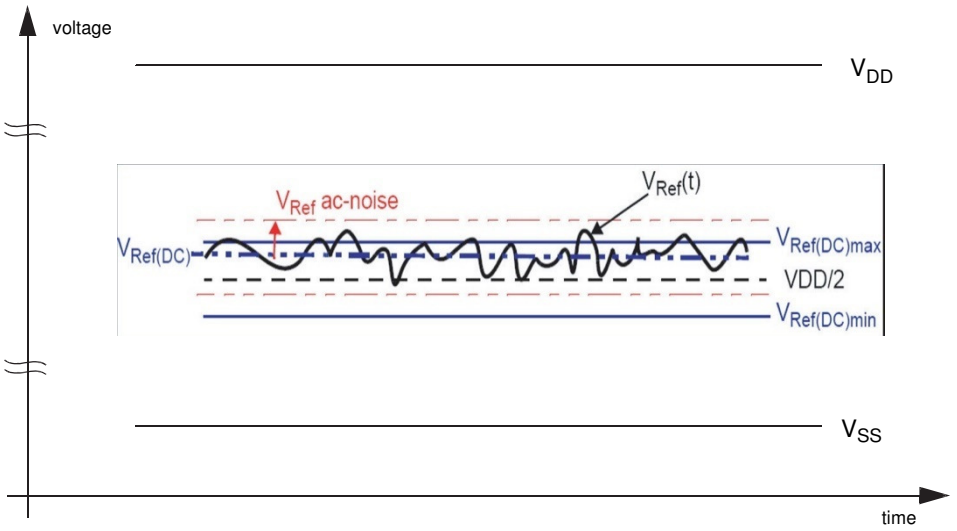
NOTE :

1. For DQ and DM : VREF = VREFDQ (DC).
2. See Overshoot and Undershoot Specifications section.
3. The AC peak noise on VREF may not allow VREF to deviate from VREFDQ (DC) by more than ±1% VDD (for reference: approx. ±15 mV).
4. For reference: approx. VDD/2 ±15 mV.
5. VIH(dc) is used as a simplified symbol for VIH.DQ(a) 1.35V : DC90, b) 1.5V : DC100)
6. VIL(dc) is used as a simplified symbol for VIL.DQ(a) 1.35V : DC90, b) 1.5V : DC100)
7. VIH(ac) is used as a simplified symbol for VIH.DQ(AC175), VIH.DQ(AC150) ; VIH.DQ(AC175) value is used when VREF + 175mV is referenced, VIH.DQ(AC150) value is used when VREF + 150mV is referenced.
8. VIL(ac) is used as a simplified symbol for VIL.DQ(AC175), VIL.DQ(AC150) ; VIL.DQ(AC175) value is used when VREF - 175mV is referenced, VIL.DQ(AC150) value is used when VREF - 150mV is referenced.

VREF Tolerances

The dc-tolerance limits and ac-noise limits for the reference voltages VREFCA and VREFDQ are illustrate in figure VREF(DC) tolerance and VREF AC-Noise limits. It shows a valid reference voltage VREF(t) as a function of time. (VREF stands for VREFCA and VREFDQ likewise).

VREF(DC) is the linear average of VREF(t) over a very long period of time (e.g. 1 sec). This average has to meet the min/max requirement in Table of “Single-Ended AC and DC Input Levels for Command and Address”. Furthermore VREF(t) may temporarily deviate from VREF(DC) by no more than +/- 1% VDD.



VREF(DC) tolerance and VREF AC-Noise limits

The voltage levels for setup and hold time measurements VIH(AC), VIH(DC), VIL(AC) and VIL(DC) are dependent on VREF.

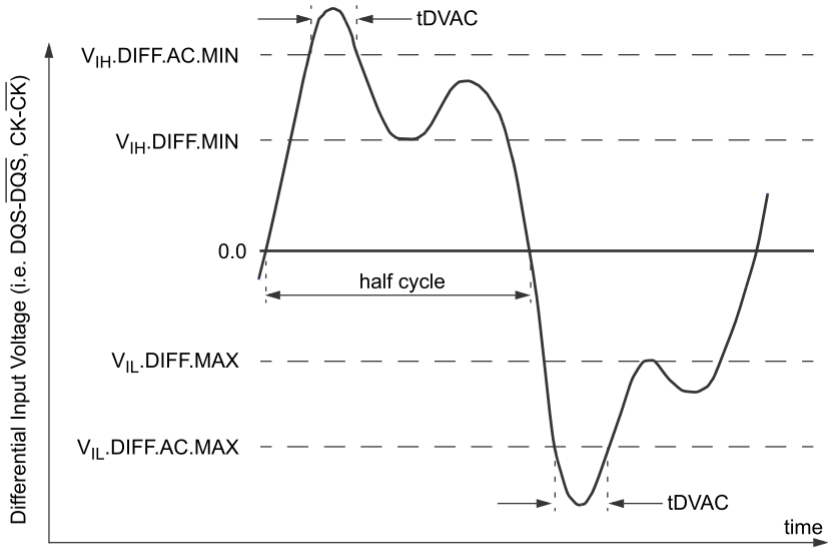
"VREF" shall be understood as VREF(DC), as defined in figure above, VREF(DC) tolerance and VREF AC- Noise limits.

This clarifies, that DC-variations of VREF affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. System timing and voltage budgets need to account for VREF(DC) deviations from the optimum position within the data-eye of the input signals.

This also clarifies that the DRAM setup/hold specification and derating values need to include time and volt- age associated with VREF AC-noise. Timing and voltage effects due to AC-noise on VREF up to the speci- fied limit (+/- 1% of VDD) are included in DRAM timings and their associated deratings.

AC and DC Logic Input Levels for Differential Signals

Differential signals definition



Definition of differential ac-swing and "time above ac level" tDVAC

Differential swing requirement for clock (CK - $\overline{CK}$) and strobe (DQS - $\overline{DQS}$)

Differential AC and DC Input Levels (1.35V)

Symbol	Parameter	Min	Max	Units	Notes
VIHdiff	Differential input high	+0.18	NOTE 3	V	1
VILdiff	Differential input low	NOTE 3	-0.18	V	1
VIHdiff(AC)	Differential input high AC	2 x (VIH(AC) - VREF)	NOTE 3	V	2
VILdiff(AC)	Differential input low AC	NOTE 3	2 x (VIL(AC) - VREF)	V	2

Differential AC and DC Input Levels(1.5V)

Symbol	Parameter	Min	Max	Units	Notes
VIHdiff	Differential input high	+0.2	NOTE 3	V	1
VILdiff	Differential input low	NOTE 3	-0.2	V	1
VIHdiff(AC)	Differential input high AC	2 x (VIH(AC) - VREF)	NOTE 3	V	2
VILdiff(AC)	Differential input low AC	NOTE 3	2 x (VIL(AC) - VREF)	V	2

NOTE :

1. Used to define a differential signal slew-rate.
2. for CK - $\overline{CK}$ use VIH/VIL(AC) of address/command and VREFCA; for strobes (DQS, $\overline{DQS}$) use VIH/VIL(AC) of DQs and VREFDQ; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.
3. These values are not defined, however the single-ended signals CK, $\overline{CK}$, DQS, $\overline{DQS}$ need to be within the respective limits (VIH(DC) max, VIL(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to "Overshoot and Undershoot specification".

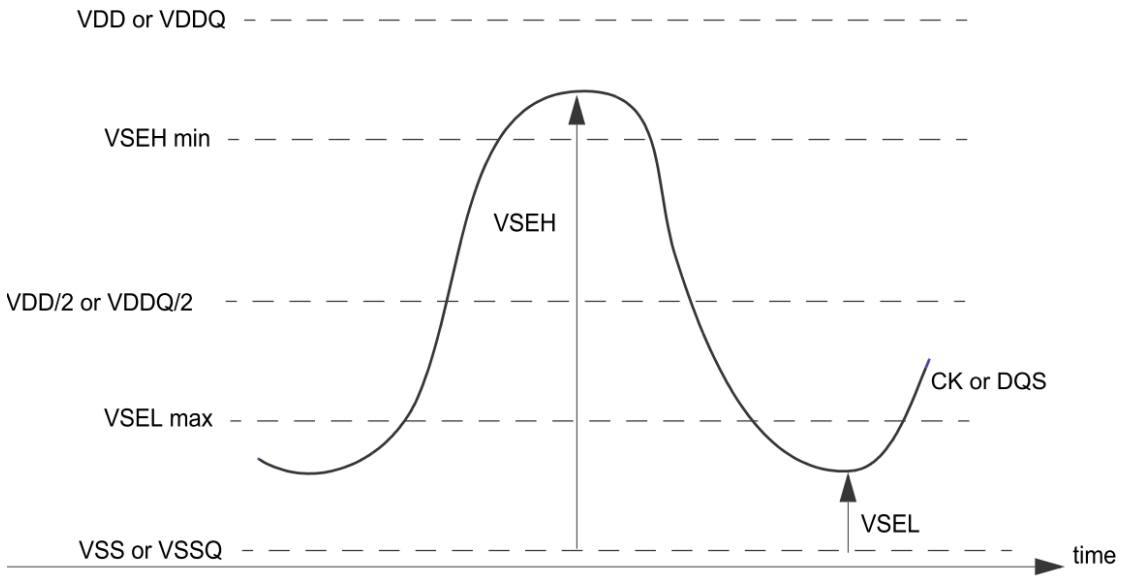
Single-ended requirements for differential signals

Each individual component of a differential signal (CK, DQS, $\overline{CK}$, $\overline{DQS}$) has also to comply with certain requirements for single-ended signals.

CK and $\overline{CK}$ have to approximately reach VSEH min / VSEL max [approximately equal to the AC-levels (VIH(AC) / VIL(AC)) for Address/command signals] in every half-cycle.

DQS, $\overline{DQS}$ have to reach VSEH min / VSEL max [approximately the ac-levels (VIH(AC) / VIL(AC)) for DQ signals] in every half-cycle proceeding and following a valid transition.

Note that the applicable AC-levels for Address/command and DQ's might be different per speed-bin etc. E.g. if VIH150(AC) / VIL150(AC) is used for Address/command signals, then these AC-levels apply also for the single-ended components of differential CK and $\overline{CK}$



Single-ended requirement for differential signals

Note that while Address/command and DQ signal requirements are with respect to VREF, the single-ended components of differential signals have a requirement with respect to VDD/2; this is nominally the same. The transition of single-ended signals through the AC-levels is used to measure setup time. For single- ended components of differential signals the requirement to reach VSEL max, VSEH min has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

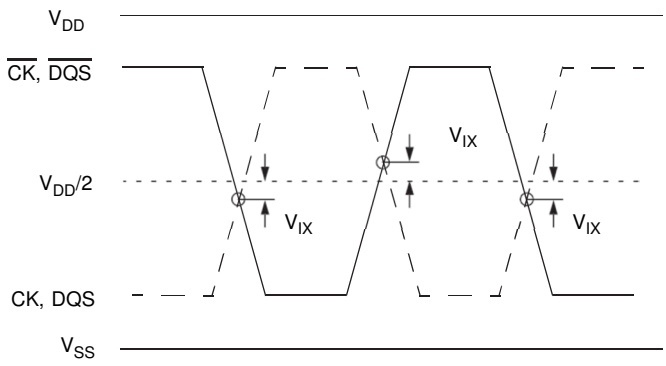
Single-ended levels for CK, DQS, $\overline{CK}$, $\overline{DQS}$

Symbol	Parameter	Min	Max	Units	Notes
VSEH	Single-ended high-level for strobes	(VDD/2) + 0.175	NOTE 3	V	1,2
	Single-ended high-level for $\overline{CK}$, CK	(VDD/2) + 0.175	NOTE 3	V	1,2
VSEL	Single-ended low-level for strobes	NOTE 3	(VDD/2) - 0.175	V	1,2
	Single-ended low-level for $\overline{CK}$, CK	NOTE 3	(VDD/2) - 0.175	V	1,2

NOTE :

1. For CK, $\overline{CK}$ use VIH/VIL(AC) of address/command; for strobes (DQS, $\overline{DQS}$) use VIH/VIL(AC) of DQs.
2. VIH(AC)/VIL(AC) for DQs is based on VREFDQ; VIH(AC)/VIL(AC) for address/command is based on VREFCA; if a reduced AC-high or AC-low level is used for a signal group, then the reduced level applies also here.
3. These values are not defined, however the single-ended components of differential signals CK, $\overline{CK}$, DQS, $\overline{DQS}$ need to be within the respective limits (VIH(DC) max, VIL(DC) min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to "Overshoot and Undershoot specifications".

To guarantee tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross point voltage of differential input signals (CK, $\overline{CK}$ and DQS, $\overline{DQS}$) must meet the requirements in below table. The differential input cross point voltage VIX is measured from the actual cross point of true and complement signal to the mid level between of VDD and VSS.



VIX Definition

Cross point voltage for differential input signals (CK, DQS): 1.35V

Symbol	Parameter	Min	Max	Units	Notes
VIX	Differential Input Cross Point Voltage relative to VDD/2 for CK, $\overline{CK}$	-150	150	mV	1
VIX	Differential Input Cross Point Voltage relative to VDD/2 for DQS, $\overline{DQS}$	-150	150	mV	1

NOTE :1. Extended range for VIX is only allowed for clock and if single-ended clock input signals CK and $\overline{CK}$ are monotonic, have a single-ended swing VSEL / VSEH of at least VDD/2 +/- 250 mV, and the differential slew rate of CK-$\overline{CK}$ is larger than 3 V/ ns. Refer to the table of Cross point voltage for differential input signals (CK, DQS) for VSEL and VSEH standard values.

Cross point voltage for differential input signals (CK, DQS): 1.5V

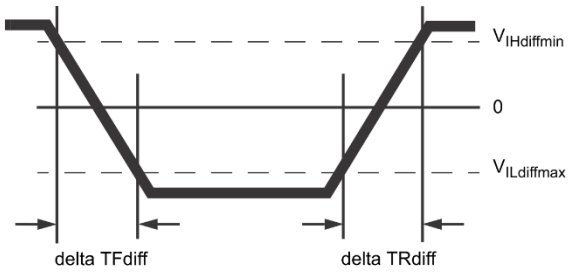
Symbol	Parameter	Min	Max	Units	Notes
VIX	Differential Input Cross Point Voltage relative to VDD/2 for CK, $\overline{CK}$	-150	150	mV	
		-175	175	mV	1
VIX	Differential Input Cross Point Voltage relative to VDD/2 for DQS, $\overline{DQS}$	-150	150	mV	

NOTE :1. Extended range for VIX is only allowed for clock and if single-ended clock input signals CK and $\overline{CK}$ are mono- tonic, have a single-ended swing VSEL / VSEH of at least VDD/2 +/- 250 mV, and the differential slew rate of CK-$\overline{CK}$ is larger than 3 V/ ns. Refer to the table of Cross point voltage for differential input signals (CK, DQS) for VSEL and VSEH standard values.

Differential input slew rate definition

Description	Measured		Defined by
	From	To	
Differential input slew rate for rising edge (CK-$\overline{CK}$ and DQS-$\overline{DQS}$)	VILdiff (max)	VIHdiff (min)	$\frac{\text{VIHdiff (min) - VILdiff (max)}}{\text{Delta TRdiff}}$
Differential input slew rate for falling edge (CK-$\overline{CK}$ and DQS-$\overline{DQS}$)	VIHdiff (min)	VILdiff (max)	$\frac{\text{VIHdiff (min) - VILdiff (max)}}{\text{Delta TFdiff}}$

NOTE : The differential signal (i.e. CK - $\overline{CK}$ and DQS - $\overline{DQS}$) must be linear between these thresholds.



Differential Input Slew Rate definition for DQS, $\overline{DQS}$, and CK, $\overline{CK}$

IDD Specification

VDD, VDDQ = 1.35V (1.283V to 1.45V)

Conditions	Symbol	Data rate (Mbps)	IDD max	Unit
			X16	
Operating One Bank Active-Precharge Current; CKE: High; External clock: On; tCK, nRC, nRAS, CL: see timing used table; BL: 8; AL: 0; : High between ACT and PRE; Command, Address: partially toggling; Data IO: FLOATING; DM:stable at 0; Bank Activity: Cycling with one bank active at a time; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	IDD0	1866 1600 1333	75 70 65	mA
Operating One Bank Active-Read-Precharge Current; CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, CL: see timing used table; BL: 81; AL: 0; : High between ACT, RD and PRE; Command, Address, Data IO: partially toggling; DM: stable at 0; Bank Activity: Cycling with one bank active at a time; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	IDD1	1866 1600 1333	85 80 75	mA
Precharge Power-Down Current Slow Exit; CKE: Low; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; : stable at 1; Command, Address: stable at 0; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0; Precharge Power Down Mode: Slow Exit	IDD2P0	1866 1600 1333	15 15 15	mA
Precharge Power-Down Current Fast Exit; CKE: Low; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; : stable at 1; Command, Address: stable at 0; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0; Precharge Power Down Mode: Fast Exit	IDD2P1	1866 1600 1333	25 22 20	mA
Precharge Standby Current; CKE: High; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; : stable at 1; Command, Address: partially toggling; Data IO: FLOATING; DM:stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	IDD2N	1866 1600 1333	40 35 30	mA
Precharge Quiet Standby Current; CKE: High; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; : stable at 1; Command, Address: stable at 0; Data IO: FLOAT- ING; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	IDD2Q	1866 1600 1333	40 35 30	mA

Conditions	Symbol	Data rate (Mbps)	IDD max X16	Unit
Active Power-Down Current; CKE: Low; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; : stable at 1; Command, Address: stable at 0; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	IDD3P	1866 1600 1333	40 35 30	mA
Active Standby Current; CKE: High; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; : stable at 1; Command, Address: partially toggling; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	IDD3N	1866 1600 1333	55 55 53	mA
Operating Burst Read Current; CKE: High; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; : High between RD; Command, Address: partially toggling; Data IO: seamless read data burst with different data between one burst and the next one; DM: stable at 0; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,...; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	IDD4R	1866 1600 1333	160 155 150	mA
Operating Burst Write Current; CKE: High; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; : High between WR; Command, Address: partially toggling; Data IO: seamless write data burst with different data between one burst and the next one; DM: stable at 0; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2, ... ; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at HIGH	IDD4W	1866 1600 1333	170 160 150	mA
Burst Refresh Current; CKE: High; External clock: On; tCK, CL, nRFC: see timing used table; BL: 8; AL: 0; : High between REF; Command, Address: partially toggling; Data IO: FLOATING; DM:stable at 0; Bank Activity: REF command every nRFC; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	IDD5B	1866 1600 1333	150 145 140	mA
Self Refresh Current: Normal Temperature Range; TCASE: 0-85°C; Auto Self-Refresh (ASR): Disabled; Self-Refresh Temperature Range (SRT): Normal; CKE: Low; External clock: Off; CK and CK: LOW; CL: see timing used table; BL: 8; AL: 0; CS, Command, Address, Data IO: FLOATING; DM: stable at 0; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: FLOATING	IDD6	1866 1600 1333	15 15 15	mA
Self Refresh Current: Extended Temperature Range; TCASE: 0-95°C; Auto Self-Refresh (ASR): Disabled; Self-Refresh Temperature Range (SRT): Extended; CKE: Low; External clock: Off; CK and CK: LOW; CL: see timing used table; BL: 8; AL: 0; CS, Command, Address, Data IO: FLOATING; DM: stable at 0; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: FLOATING	IDD6ET	1866 1600 1333	20 20 20	mA

Conditions	Symbol	Data rate (Mbps)	IDD max X16	Unit
Operating Bank Interleave Read Current; CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL: see timing used table; BL: 8; AL: CL-1; CS: High between ACT and RDA; Command, Address: partially toggling; Data IO: read data bursts with different data between one burst and the next one; DM: stable at 0; Bank Activity: two times interleaved cycling through banks (0, 1, ... 7) with different addressing; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	IDD7	1866 1600 1333	250 240 230	mA
RESET Low Current; RESET: Low; External clock: off; CK and CK: LOW; CKE: FLOATING; CS, Command, Address, Data IO: FLOATING; ODT Signal : FLOATING	IDD8	1866 1600 1333	14 14 14	mA

NOTE :

1) Burst Length: BL8 fixed by MRS: set MR0 A[1,0]=00B
2) Output Buffer Enable: set MR1 A[12] = 0B; set MR1 A[5,1] = 01B; RTT_Nom enable: set MR1 A[9,6,2] = 011B; RTT_Wr enable: set MR2 A[10,9] = 10B
3) Precharge Power Down Mode: set MR0 A12=0B for Slow Exit or MR0 A12=1B for Fast Exit
4) Auto Self-Refresh (ASR): set MR2 A6 = 0B to disable or 1B to enable feature
5) Self-Refresh Temperature Range (SRT): set MR2 A7=0B for normal or 1B for extended temperature range
6) Refer to DRAM supplier data sheet and/or DIMM SPD to determine if optional features or requirements are supported by DDR3 SDRAM
7) Read Burst type: Nibble Sequential, set MR0 A[3]=0B

Timing used for IDD and IDDQ Measured - Loop Patterns

Speed	DDR3-1333	DDR3-1600	DDR3-1866	Unit
CL-nRCD-nRP	**9-9-9**	**11-11-11**	**13-13-13**	
tCKmin	1.5	1.25	1.071	ns
CL	9	11	13	nCK
tRCDmin	9	11	13	nCK
tRCmin	33	39	45	nCK
tRASmin	24	28	32	nCK
tRPmin	9	11	13	nCK
tFAW (2KB page size)	30	32	33	nCK
tRRD (2KB page size)	5	6	6	nCK
tRFC	107	128	150	nCK

DDR3-1333 Speed Bins

Speed Bin				-15E (DDR3-1333)		Unit	Notes
CL-nRCD-nRP				9-9-9			
Parameter			Symbol	Min	Max		
Internal read command to first data			tAA	13.5	20	ns	
Active to read or write delay time			tRCD	13.5	-	ns	
Precharge command period			tRP	13.5	-	ns	
Active to active/auto-refresh command time			tRC	49.5	-	ns	
Active to precharge command period			tRAS	36	9 * tREFI	ns	
Average Clock Cycle Time	CL = 5	CWL = 5	tCK(avg)	3.0	3.3	ns	1,2,3,6
		CWL = 6,7	tCK(avg)	Reserved	Reserved	ns	4
	CL = 6	CWL = 5	tCK(avg)	2.5	3.3	ns	1,2,3,6
		CWL = 6	tCK(avg)	Reserved	Reserved	ns	4
		CWL = 7	tCK(avg)	Reserved	Reserved	ns	4
	CL = 7	CWL = 5	tCK(avg)	Reserved	Reserved	ns	4
		CWL = 6	tCK(avg)	1.875	< 2.5	ns	1,2,3,6
		CWL = 7	tCK(avg)	Reserved	Reserved	ns	4
	CL = 8	CWL = 5	tCK(avg)	Reserved	Reserved	ns	4
		CWL = 6	tCK(avg)	1.875	< 2.5	ns	1,2,3,6
		CWL = 7	tCK(avg)	Reserved	Reserved	ns	4
	CL = 9	CWL = 5, 6	tCK(avg)	Reserved	Reserved	ns	4
		CWL = 7	tCK(avg)	1.5	< 1.875	ns	1,2,3
	CL = 10	CWL = 5, 6	tCK(avg)	Reserved	Reserved	ns	4
		CWL = 7	tCK(avg)	Reserved	Reserved	ns	4
Supported CL setting				5, 6, 7, 8, 9, 10		nCK	
Supported CWL setting				5, 6, 7		nCK	

DDR3-1600 Speed Bins

Speed Bin				- 125 (DDR3-1600)		Unit	Notes
CL-nRCD-nRP				11-11-11			
Parameter			Symbol	Min	Max		
Internal read command to first data			t_{AA}	13.75	20	ns	
Active to read or write delay time			t_{RCD}	13.75	-	ns	
Precharge command period			t_{RP}	13.75	-	ns	
Active to active/auto-refresh command time			t_{RC}	48.75	-	ns	
Active to precharge command period			t_{RAS}	35	9 * t_{REFI}	ns	
Average Clock Cycle Time	CL = 5	CWL = 5	$t_{CK(avg)}$	3.0	3.3	ns	1,2,3,7
		CWL = 6,7	$t_{CK(avg)}$	Reserved	Reserved	ns	4
	CL = 6	CWL = 5	$t_{CK(avg)}$	2.5	3.3	ns	1,2,3,7
		CWL = 6	$t_{CK(avg)}$	Reserved	Reserved	ns	4
		CWL = 7	$t_{CK(avg)}$	Reserved	Reserved	ns	4
	CL = 7	CWL = 5	$t_{CK(avg)}$	Reserved	Reserved	ns	4
		CWL = 6	$t_{CK(avg)}$	1.875	< 2.5	ns	1,2,3,7
		CWL = 7	$t_{CK(avg)}$	Reserved	Reserved	ns	4
	CL = 8	CWL = 5	$t_{CK(avg)}$	Reserved	Reserved	ns	4
		CWL = 6	$t_{CK(avg)}$	1.875	< 2.5	ns	1,2,3,7
		CWL = 7	$t_{CK(avg)}$	Reserved	Reserved	ns	4
	CL = 9	CWL = 5, 6	$t_{CK(avg)}$	Reserved	Reserved	ns	4
		CWL = 7	$t_{CK(avg)}$	1.5	< 1.875	ns	1,2,3,7
	CL = 10	CWL = 5, 6	$t_{CK(avg)}$	Reserved	Reserved	ns	4
		CWL = 7	$t_{CK(avg)}$	1.5	< 1.875	ns	1,2,3,7
		CWL = 8	$t_{CK(avg)}$	Reserved	Reserved	ns	4
	CL = 11	CWL = 5, 6,7	$t_{CK(avg)}$	Reserved	Reserved	ns	4
		CWL = 8	$t_{CK(avg)}$	1.25	< 1.5	ns	1,2,3
Supported CL setting				5, 6, 7, 8, 9, 10, 11		nCK	
Supported CWL setting				5, 6, 7, 8		nCK	

DDR3-1866 Speed Bins

Speed Bin				- 107 (DDR3-1866)		Unit	Notes
CL-nRCD-nRP				13-13-13			
Parameter			Symbol	Min	Max		
Internal read command to first data			t_{AA}	13.91	20	ns	
Active to read or write delay time			t_{RCD}	13.91	-	ns	
Precharge command period			t_{RP}	13.91	-	ns	
Active to active/auto-refresh command time			t_{RC}	47.91	-	ns	
Active to precharge command period			t_{RAS}	34	9 * t_{REFI}	ns	
Average Clock Cycle Time	CL = 5	CWL = 5	$t_{CK(avg)}$	Reserved	Reserved	ns	4
		CWL = 6,7,8,9	$t_{CK(avg)}$	Reserved	Reserved	ns	4
	CL = 6	CWL = 5	$t_{CK(avg)}$	2.5	3.3	ns	1,2,3,8
		CWL = 6	$t_{CK(avg)}$	Reserved	Reserved	ns	4
		CWL = 7,8,9	$t_{CK(avg)}$	Reserved	Reserved	ns	4
	CL = 7	CWL = 5	$t_{CK(avg)}$	Reserved	Reserved	ns	4
		CWL = 6	$t_{CK(avg)}$	1.875	< 2.5	ns	1,2,3,8
		CWL = 7,8,9	$t_{CK(avg)}$	Reserved	Reserved	ns	4
	CL = 8	CWL = 5	$t_{CK(avg)}$	Reserved	Reserved	ns	4
		CWL = 6	$t_{CK(avg)}$	1.875	< 2.5	ns	1,2,3,8
		CWL = 7	$t_{CK(avg)}$	Reserved	Reserved	ns	4
		CWL = 8,9	$t_{CK(avg)}$	Reserved	Reserved	ns	4
	CL = 9	CWL = 5,6	$t_{CK(avg)}$	Reserved	Reserved	ns	4
		CWL = 7	$t_{CK(avg)}$	1.5	< 1.875	ns	1,2,3,8
		CWL = 8	$t_{CK(avg)}$	Reserved	Reserved	ns	4
		CWL = 9	$t_{CK(avg)}$	Reserved	Reserved	ns	4
	CL = 10	CWL = 5,6	$t_{CK(avg)}$	Reserved	Reserved	ns	4
		CWL = 7	$t_{CK(avg)}$	1.5	< 1.875	ns	1,2,3,8
		CWL = 8	$t_{CK(avg)}$	Reserved	Reserved	ns	4
	CL = 11	CWL = 5,6,7	$t_{CK(avg)}$	Reserved	Reserved	ns	4
		CWL = 8	$t_{CK(avg)}$	1.25	< 1.5	ns	1,2,3,8
		CWL = 9	$t_{CK(avg)}$	Reserved	Reserved	ns	4
	CL = 12	CWL = 5,6,7,8	$t_{CK(avg)}$	Reserved	Reserved	ns	4
		CWL = 9	$t_{CK(avg)}$	Reserved	Reserved	ns	4
	CL = 13	CWL = 5,6,7,8	$t_{CK(avg)}$	Reserved	Reserved	ns	4
		CWL = 9	$t_{CK(avg)}$	1.07	<1.25	ns	1,2,3
Supported CL setting				6, 7, 8, 9, 10, 11, 13		nCK	
Supported CWL setting				5, 6, 7, 8, 9		nCK	

Speed Bin Table Notes

NOTE :

1. The CL setting and CWL setting result in tCK(avg) Min and tCK(avg) Max requirements. When making a selection of tCK(avg), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.

2. tCK(avg) Min limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard tCK(avg) value (2.5, 1.875, 1.5, or 1.25 ns) when calculating CL [nCK] = tAA [ns] / tCK(avg) [ns], rounding up to the next "Supported CL".

3. tCK(avg) Max limits: Calculate tCK(avg) = tAA Max / CL Selected and round the resulting tCK(avg) down to the next valid speed bin (i.e. 3.3ns or 2.5ns or 1.875 ns or 1.25 ns). This result is tCK(avg) Max corresponding to CL selected.

4. "Reserved" settings are not allowed. User must program a different value.

5. Any DDR3-1066 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to production tests but verified by design/characterization.

6. Any DDR3-1333 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to production tests but verified by design/characterization.

7. Any DDR3-1600 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to production tests but verified by design/characterization.

8. Any DDR3-1866 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to production tests but verified by design/characterization.

9. tREFI depends on operating case temperature (Tcase).

10. For devices supporting optional downshift to CL=7 and CL=9, tAA/tRCD/tRP min must be 13.125 ns or lower. SPD settings must be programmed to match. For example, DDR3-1333(CL9) devices supporting downshift to DDR3-1066(CL7) should program 13.125 ns in SPD bytes for tAAmin (Byte 16), tRCDmin (Byte 18), and tRPmin (Byte 20). DDR3-1600(CL11) devices supporting downshift to DDR3-1333(CL9) or DDR3-1066(CL7) should program 13.125 ns in SPD bytes for tAAmin (Byte16), tRCDmin (Byte 18), and tRPmin (Byte 20). Once tRP (Byte 20) is programmed to 13.125ns, tRCmin (Byte 21,23) also should be programmed accod- ingly. For example, 49.125ns, (tRASmin + tRPmin = 36ns + 13.125ns) for DDR3-1333 and 48.125ns (tRASmin + tRPmin = 35ns + 13.125ns) for DDR3-1600.
For devices supporting optional down binning to CL=11, CL=9 and CL=7, tAA/tRCD/tRPmin must be 13.125ns. SPD setting must be programed to match. For example, DDR3-1866 devices supporting down binning to DDR3-1600 or DDR3-1333 or 1066 should program 13.125ns in SPD bytes for tAAmin(byte16), tRCDmin(Byte18) and tRP-min (byte20). Once tRP (Byte20) is programmed to 13.125ns, tRCmin (Byte21,23) also should be programmed accord- ingly. For example, 47.125ns (tRASmin + tRPmin = 34ns + 13.125ns)

AC Characteristics

(VDD = 1.35V; VDDQ =1.35V)

Parameter	Symbol	- 15E (DDR3-1333)		- 125 (DDR3-1600)		Unit	Note
		Min	Max	Min	Max		
Average clock cycle time	t_{CK}(avg)	Please refer Speed Bins				ps	
Minimum clock cycle time (DLL-off mode)	t_{CK} (DLL-off)	8	-	8	-	ns	6
Average CK high level width	t_{CH}(avg)	0.47	0.53	0.47	0.53	t_{CK}(avg)	
Average CK low level width	t_{CL}(avg)	0.47	0.53	0.47	0.53	t_{CK}(avg)	
Active Bank A to Active Bank B command period for 1KB page size	t_{RRD}	6	-	6	-	ns	
		4	-	4	-	nCK	
Active Bank A to Active Bank B command period for 2KB page size	t_{RRD}	7.5	-	7.5	-	ns	
		4	-	4	-	nCK	
Four activate window for 1KB page size	t_{FAW}	30	-	30	-	ns	
Four activate window for 2KB page size	t_{FAW}	45	-	40	-	ns	
Address and Control input hold time (VIH/VIL (DC) levels)	1.35V						
	t_{IH}(base) DC90	150	-	130	-	ps	16
	1.5V						
	t_{IH}(base) DC100	140	-	120	-	ps	16
Address and Control input setup time (VIH/VIL (AC) levels)	1.35V						
	t_{IS}(base) AC160	80	-	60	-	ps	16
	1.5V						
	t_{IS}(base) AC175	65	-	45	-	ps	16
Address and Control input setup time (VIH/VIL (AC) levels)	1.35V						
	t_{IS}(base) AC135	205	-	185	-	ps	16
	1.5V						
	t_{IS}(base) AC150	190	-	170	-	ps	16,24
DQ and DM input hold time (VIH/VIL (DC) levels)	1.35V						
	t_{DH}(base) DC90	75	-	55	-	ps	17
	1.5V						
	t_{DH}(base) DC100	65	-	45	-	ps	17
DQ and DM input setup time (VIH/VIL (AC) levels)	1.35V						
	t_{DS}(base) AC160	-	-	-	-	ps	17
	1.5V						
	t_{DS}(base) AC175	-	-	-	-	ps	17

Parameter	Symbol	- 15E (DDR3-1333)		- 125 (DDR3-1600)		Unit	Note
		Min	Max	Min	Max		
DQ and DM input setup time (VIH/VIL (AC) levels)	1.35V						
	t_{DS}(base) AC135	45	-	25	-	ps	17
	1.5V						
	t_{DS}(base) AC150	30	-	10	-	ps	17
Control and Address Input pulse width for each input	t_{IPW}	620	-	560	-	ps	25
DQ and DM Input pulse width for each input	t_{DIPW}	400	-	360	-	ps	25
DQ high impedance time	t_{HZ}(DQ)	-	250	-	225	ps	13,14
DQ low impedance time	t_{LZ}(DQ)	-500	250	-450	225	ps	13,14
DQS, $\overline{DQS}$ high impedance time (RL + BL/2 reference)	t_{HZ}(DQS)	-	250	-	225	ps	13,14
DQS, $\overline{DQS}$ low impedance time (RL - 1 reference)	t_{LZ}(DQS)	-500	250	-450	225	ps	13,14
DQS, $\overline{DQS}$ to DQ Skew, per group, per access	t_{DQSQ}	-	125	-	100	ps	12,13
$\overline{CAS}$ to $\overline{CAS}$ command delay	t_{CCD}	4	-	4	-	nCK	
DQ output hold time from DQS, $\overline{DQS}$	t_{QH}	0.38	-	0.38	-	t_{CK}(avg)	12,13
DQS, DQS rising edge output access time from rising CK, $\overline{CK}$	t_{DQSCK}	-255	255	-225	225	ps	12,13
DQS latching rising transitions to associated clock edges	t_{DQSS}	-0.25	0.25	-0.27	0.27	t_{CK}(avg)	
DQS falling edge hold time from rising CK	t_{DSH}	0.2	-	0.18	-	t_{CK}(avg)	29
DQS falling edge setup time to rising CK	t_{DSS}	0.2	-	0.18	-	t_{CK}(avg)	29
DQS input high pulse width	t_{DQSH}	0.45	0.55	0.45	0.55	t_{CK}(avg)	27,28
DQS input low pulse width	t_{DQSL}	0.45	0.55	0.45	0.55	t_{CK}(avg)	26,28
DQS output high time	t_{QSH}	0.40	-	0.40	-	t_{CK}(avg)	12,13
DQS output low time	t_{QSL}	0.40	-	0.40	-	t_{CK}(avg)	12,13
Mode register set command cycle time	t_{MRD}	4	-	4	-	nCK	
Mode register set command update delay	t_{MOD}	15	-	15	-	ns	
		12	-	12	-	nCK	
Read preamble time	t_{RPRE}	0.9	-	0.9	-	t_{CK}(avg)	13,19
Read postamble time	t_{RPST}	0.3	-	0.3	-	t_{CK}(avg)	11,13
Write preamble time	t_{WPRE}	0.9	-	0.9	-	t_{CK}(avg)	1
Write postamble time	t_{WPST}	0.3	-	0.3	-	t_{CK}(avg)	1
Write recovery time	t_{WR}	15	-	15	-	ns	
Auto precharge write recovery + Precharge time	t_{DAL}(min)	WR + roundup [tRP / tCK(avg)]				nCK	

Parameter	Symbol	- 15E (DDR3-1333)		- 125 (DDR3-1600)		Unit	Note
		Min	Max	Min	Max		
Multi-purpose register recovery time	t_{MPRR}	1	-	1	-	nCK	22
Internal write to read command delay	t_{WTR}	7.5	-	7.5	-	ns	18
		4	-	4	-	nCK	18
Internal read to precharge command delay	t_{RTP}	7.5	-	7.5	-	ns	
		4	-	4	-	nCK	
Minimum CKE low width for Self-refresh entry to exit timing	t_{CKESR}	t_{CKE}(min) +1nCK	-	t_{CKE}(min) +1nCK	-		
Valid clock requirement after Self- refresh entry or Power-down entry	t_{CKSRE}	10	-	10	-	ns	
		5	-	5	-	nCK	
Valid clock requirement before Self- refresh exit or Power-down exit	t_{CKSRX}	10	-	10	-	ns	
		5	-	5	-	nCK	
Exit Self-refresh to commands not requiring a locked DLL	t_{XS}	t_{RFC}(min) +10	-	t_{RFC}(min) +10	-	ns	
		5	-	5	-	nCK	
Exit Self-refresh to commands requiring a locked DLL	t_{XSDLL}	t_{DLLK} (min)	-	t_{DLLK} (min)	-	nCK	
Auto-refresh to Active/Auto-refresh command time	t_{RFC}	300	-	300	-	ns	
Average Periodic Refresh Interval Commercial: 0°C ≤ Tc ≤ +85°C Industrial: -40°C ≤ Tc ≤ +85°C	t_{REFI}	-		7.8		µs	
Average Periodic Refresh Interval Commercial: +85°C < Tc ≤ +95°C Industrial: +85°C < Tc ≤ +95°C	t_{REFI}	-		3.9		µs	
CKE minimum high and low pulse width	t_{CKE}	5.625	-	5	-	ns	
		3	-	3	-	nCK	
Exit reset from CKE high to a valid command	t_{XPR}	t_{RFC}(min) +10	-	t_{RFC}(min) +10	-	ns	
		5	-	5	-	nCK	
DLL locking time	t_{DLLK}	512	-	512	-	nCK	
Power-down entry to exit time	t_{PD}	t_{CKE}(min)	9*t_{REFI}	t_{CKE}(min)	9*t_{REFI}		15
Exit precharge power-down with DLL frozen to commands requiring a locked DLL	t_{XPDLL}	24	-	24	-	ns	2
		10	-	10	-	nCK	2
Exit power-down with DLL on to any valid command; Exit precharge power-down with DLL frozen to commands not requiring a locked DLL	t_{XP}	6	-	6	-	ns	
		3	-	3	-	nCK	
Command pass disable delay	t_{CPDED}	1	-	1	-	nCK	
Timing of ACT command to Power-down entry	$t_{ACTPDEN}$	1	-	1	-	nCK	20
Timing of PRE command to Power-down entry	t_{PRPDEN}	1	-	1	-	nCK	20
Timing of RD/RDA command to Power-down entry	t_{RDPDEN}	RL+4+1	-	RL+4+1	-	nCK	

Parameter	Symbol	- 15E (DDR3-1333)		- 125 (DDR3-1600)		Unit	Note
		Min	Max	Min	Max		
Timing of WR command to Power-down entry (BL8OTF, BL8MRS, BL4OTF)	t_{WRPDEN} (min)	WL + 4 + [tWR/tCK(avg)]				nCK	9
Timing of WR command to Power-down entry (BC4MRS)	t_{WRPDEN} (min)	WL + 2 + [tWR/tCK(avg)]				nCK	9
Timing of WRA command to Power-down entry (BL8OTF, BL8MRS, BL4OTF)	tWRAPDEN	WL+4 +WR+1	-	WL+4 +WR+1	-	nCK	10
Timing of WRA command to Power-down entry (BC4MRS)	t WRAPDEN	WL+2 +WR+1	-	WL+2 +WR+1	-	nCK	10
Timing of REF command to Power-down entry	$t_{REFPDEN}$	1	-	1	-	nCK	20,21
Timing of MRS command to Power-down entry	t MRSPDEN	t_{MOD} (min)	-	t_{MOD} (min)	-		
RTT turn-on	t_{AON}	-250	250	-225	225	ps	7
Asynchronous RTT turn-on delay (Power-down with DLL frozen)	t_{AONPD}	2	8.5	2	8.5	ns	
RTT_Nom and RTT_WR turn-off time from ODTLoff reference	t	0.3	0.7	0.3	0.7	t_{CK}(avg)	8
Asynchronous RTT turn-off delay (Power-down with DLL frozen)	t_{AOFPD}	2	8.5	2	8.5	ns	
ODT high time without write command or with write command and BC4	ODTH4	4	-	4	-	nCK	
ODT high time with Write command and BL8	ODTH8	6	-	6	-	nCK	
RTT dynamic change skew	t_{ADC}	0.3	0.7	0.3	0.7	t_{CK}(avg)	
Power-up and reset calibration time	t_{ZQinit}	512	-	512	-	nCK	
Normal operation full calibration time	t_{ZQoper}	256	-	256	-	nCK	
Normal operation short calibration time	t_{ZQCS}	64	-	64	-	nCK	23
First DQS pulse rising edge after write leveling mode is programmed	t_{WLMRD}	40	-	40	-	nCK	3
DQS, $\overline{DQS}$ delay after write leveling mode is pro-grammed	$t_{WLDQSEN}$	25	-	25	-	nCK	3
Write leveling setup time from rising CK, $\overline{CK}$ crossing to rising DQS, $\overline{DQS}$ crossing	t_{WLS}	195	-	165	-	ps	
Write leveling hold time from rising DQS, $\overline{DQS}$ crossing to rising CK, $\overline{CK}$ crossing	t_{WLH}	195	-	165	-	ps	
Write leveling output delay	t_{WLO}	0	9	0	7.5	ns	
Write leveling output error	t_{WLOE}	0	2	0	2	ns	
Absolute clock period	t_{CK}(abs)	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	ps	
Absolute clock high pulse width	t_{CH}(abs)	0.43	-	0.43	-	t_{CK}(avg)	30
Absolute clock low pulse width	t_{CL}(abs)	0.43	-	0.43	-	t_{CK}(avg)	31
Clock period jitter	t_{JIT}(per)	-80	80	-70	70	ps	
Clock period jitter during DLL locking period	t_{JIT}(per,lck)	-70	70	-60	60	ps	
Cycle to cycle period jitter	t_{JIT}(cc)	-	160	-	140	ps	

Parameter	Symbol	- 15E (DDR3-1333)		- 125 (DDR3-1600)		Unit	Note
		Min	Max	Min	Max		
Cycle to cycle period jitter during DLL locking period	t_{JIT}(cc,lck)	-	140	-	120	ps	
Cumulative error across 2 cycles	t_{ERR}(2per)	-118	118	-103	103	ps	
Cumulative error across 3 cycles	t_{ERR}(3per)	-140	140	-122	122	ps	
Cumulative error across 4 cycles	t_{ERR}(4per)	-155	155	-136	136	ps	
Cumulative error across 5 cycles	t_{ERR}(5per)	-168	168	-147	147	ps	
Cumulative error across 6 cycles	t_{ERR}(6per)	-177	177	-155	155	ps	
Cumulative error across 7 cycles	t_{ERR}(7per)	-186	186	-163	163	ps	
Cumulative error across 8 cycles	t_{ERR}(8per)	-193	193	-169	169	ps	
Cumulative error across 9 cycles	t_{ERR}(9per)	-200	200	-175	175	ps	
Cumulative error across 10 cycles	t_{ERR}(10per)	-205	205	-180	180	ps	
Cumulative error across 11 cycles	t_{ERR}(11per)	-210	210	-184	184	ps	
Cumulative error across 12 cycles	t_{ERR}(12per)	-215	215	-188	188	ps	
Cumulative error across n = 13,14,...49,50 cycles	t_{ERR}(nper)	$t_{ERR}(nper)min = (1 + 0.68ln(n))*t_{JIT}(per)min$ $t_{ERR}(nper)max = (1 + 0.68ln(n))*t_{JIT}(per)max$				ps	32

Parameter	Symbol	- 107 (DDR3-1866)		Unit	Note
		Min	Max		
Average clock cycle time	t_{CK}(avg)	Please refer Speed Bins		ps	
Minimum clock cycle time (DLL-off mode)	t_{CK} (DLL-off)	8	-	ns	6
Average CK high level width	t_{CH}(avg)	0.47	0.53	t_{CK}(avg)	
Average CK low level width	t_{CL}(avg)	0.47	0.53	t_{CK}(avg)	
Active Bank A to Active Bank B command period for 2KB page size	t_{RRD}	6	-	ns	
		4	-	nCK	
Four activate window for 2KB page size	t_{FAW}	35		ns	
Address and Control input hold time (VIH/VIL (DC) levels)	1.35V				
	t_{IH}(base) DC90	110	-	ps	16
	1.5V				
	t_{IH}(base) DC100	100	-	ps	16
Address and Control input setup time (VIH/VIL (AC) levels)	1.35V				
	t_{IS}(base) AC125	150	-	ps	16
	1.5V				
	t_{IS}(base) AC125	150	-	ps	16
Address and Control input setup time (VIH/VIL (AC) levels)	1.35V				
	t_{IS}(base) AC135	65	-	ps	16
	1.5V				
	t_{IS}(base) AC150	65	-	ps	16,24
DQ and DM input hold time (VIH/VIL (DC) levels)	1.35V				
	t_{DH}(base) DC90	75	-	ps	17
	1.5V				
	t_{DH}(base) DC100	70	-	ps	17
DQ and DM input setup time (VIH/VIL (AC) levels)	1.35V				
	t_{DS}(base) AC130	70	-	ps	17
	1.5V				
	t_{DS}(base) AC135	68	-	ps	17
Control and Address Input pulse width for each input	t_{IPW}	535	-	ps	25
DQ and DM Input pulse width for each input	t_{DIPW}	320	-	ps	25

Parameter	Symbol	- 107 (DDR3-1866)		Unit	Note
		Min	Max		
DQ high impedance time	t_{HZ}(DQ)	-	195	ps	13,14
DQ low impedance time	t_{LZ}(DQ)	-390	195	ps	13,14
DQS, $\overline{DQS}$ high impedance time (RL + BL/2 reference)	t_{HZ}(DQS)	-	195	ps	13,14
DQS, $\overline{DQS}$ low impedance time (RL - 1 reference)	t_{LZ}(DQS)	-390	195	ps	13,14
DQS, $\overline{DQS}$ to DQ Skew, per group, per access	t_{DQSQ}	-	85	ps	12,13
$\overline{CAS}$ to $\overline{CAS}$ command delay	t_{CCD}	4	-	nCK	
DQ output hold time from DQS, $\overline{DQS}$	t_{QH}	0.38	-	t_{CK}(avg)	12,13
DQS, DQS rising edge output access time from rising CK, $\overline{CK}$	t_{DQSCK}	-195	195	ps	12,13
DQS latching rising transitions to associated clock edges	t_{DQSS}	-0.27	0.27	t_{CK}(avg)	
DQS falling edge hold time from rising CK	t_{DSH}	0.18	-	t_{CK}(avg)	29
DQS falling edge setup time to rising CK	t_{DSS}	0.18	-	t_{CK}(avg)	29
DQS input high pulse width	t_{DQSH}	0.45	0.55	t_{CK}(avg)	27,28
DQS input low pulse width	t_{DQSL}	0.45	0.55	t_{CK}(avg)	26,28
DQS output high time	t_{QSH}	0.40	-	t_{CK}(avg)	12,13
DQS output low time	t_{QSL}	0.40	-	t_{CK}(avg)	12,13
Mode register set command cycle time	t_{MRD}	4		nCK	
Mode register set command update delay	t_{MOD}	15	-	ns	
		12	-	nCK	
Read preamble time	t_{RPRE}	0.9	-	t_{CK}(avg)	13,19
Read postamble time	t_{RPST}	0.3	-	t_{CK}(avg)	11,13
Write preamble time	t_{WPRE}	0.9	-	t_{CK}(avg)	1
Write postamble time	t_{WPST}	0.3	-	t_{CK}(avg)	1
Write recovery time	t_{WR}	15	-	ns	
Auto precharge write recovery + Precharge time	t_{DAL}(min)	WR + roundup [tRP / tCK(avg)]		nCK	
Multi-purpose register recovery time	t_{MPRR}	1	-	nCK	22
Internal write to read command delay	t_{WTR}	7.5	-	ns	18
		4	-	nCK	18
Internal read to precharge command delay	t_{RTP}	7.5	-	ns	
		4	-	nCK	
Minimum CKE low width for Self-refresh entry to exit timing	t_{CKESR}	t_{CKE}(min)+1nCK	-		
Valid clock requirement after Self- refresh entry or Power-down entry	t_{CKSRE}	10	-	ns	
		5	-	nCK	

Parameter	Symbol	- 107 (DDR3-1866)		Unit	Note
		Min	Max		
Valid clock requirement before Self- refresh exit or Power-down exit	t_{CKSRX}	10	-	ns	
		5	-	nCK	
Exit Self-refresh to commands not requiring a locked DLL	t_{XS}	t_{RFC}(min)+10	-	ns	
		5	-	nCK	
Exit Self-refresh to commands requiring a locked DLL	t_{XSDLL}	t_{DLLK}(min)	-	nCK	
Auto-refresh to Active/Auto-refresh command time	t_{RFC}	300	-	ns	
Average Periodic Refresh Interval Commercial: 0°C ≤ Tc ≤ +85°C Industrial: -40°C ≤ Tc ≤ +85°C	t_{REFI}	-	7.8	µs	
Average Periodic Refresh Interval Commercial: +85°C < Tc ≤ +95°C Industrial: +85°C < Tc ≤ +95°C	t_{REFI}	-	3.9	µs	
CKE minimum high and low pulse width	t_{CKE}	5	-	ns	
		3	-	nCK	
Exit reset from CKE high to a valid command	t_{XPR}	tRFC(min)+10	-	ns	
		5	-	nCK	
DLL locking time	t_{DLLK}	512	-	nCK	
Power-down entry to exit time	t_{PD}	tCKE(min)	9*tREFI		15
Exit precharge power-down with DLL frozen to commands requiring a locked DLL	t_{XPDLL}	24	-	ns	2
		10	-	nCK	2
Exit power-down with DLL on to any valid command; Exit precharge power-down with DLL frozen to commands not requiring a locked DLL	t_{XP}	6	-	ns	
		3	-	nCK	
Command pass disable delay	t_{CPDED}	2	-	nCK	
Timing of ACT command to Power-down entry	$t_{ACTPDEN}$	1	-	nCK	20
Timing of PRE command to Power-down entry	t_{PRPDEN}	1	-	nCK	20
Timing of RD/RDA command to Power-down entry	t_{RDPDEN}	RL+4+1	-	nCK	
Timing of WR command to Power-down entry (BL8OTF, BL8MRS, BL4OTF)	t_{WRPDEN} (min)	WL + 4 + [tWR/tCK(avg)]		nCK	9
Timing of WR command to Power-down entry (BC4MRS)	t_{WRPDEN} (min)	WL + 2 + [tWR/tCK(avg)]		nCK	9
Timing of WRA command to Power-down entry (BL8OTF, BL8MRS, BL4OTF)	tWRAPDEN	WL+4 +WR+1	-	nCK	10
Timing of WRA command to Power-down entry (BC4MRS)	t WRAPDEN	WL+2 +WR+1	-	nCK	10
Timing of REF command to Power-down entry	$t_{REFPDEN}$	1	-	nCK	20,21
Timing of MRS command to Power-down entry	t MRSPDEN	t_{MOD} (min)	-		

Parameter	Symbol	- 107 (DDR3-1866)		Unit	Note
		Min	Max		
RTT turn-on	t_{AON}	-195	195	ps	7
Asynchronous RTT turn-on delay (Power-down with DLL frozen)	t_{AONPD}	2	8.5	ns	
RTT_Nom and RTT_WR turn-off time from ODTLoff reference	t	0.3	0.7	t_{CK}(avg)	8
Asynchronous RTT turn-off delay (Power-down with DLL frozen)	t_{AOFPD}	2	8.5	ns	
ODT high time without write command or with write command and BC4	ODTH4	4	-	nCK	
ODT high time with Write command and BL8	ODTH8	6	-	nCK	
RTT dynamic change skew	t_{ADC}	0.3	0.7	t_{CK}(avg)	
Power-up and reset calibration time	t_{ZQinit}	512	-	nCK	
Normal operation full calibration time	t_{ZQoper}	256	-	nCK	
Normal operation short calibration time	t_{ZQCS}	64	-	nCK	23
First DQS pulse rising edge after write leveling mode is programmed	t_{WLMRD}	40	-	nCK	3
DQS, $\overline{DQS}$ delay after write leveling mode is pro-grammed	$t_{WLDQSEN}$	25	-	nCK	3
Write leveling setup time from rising CK, $\overline{CK}$ crossing to rising DQS, $\overline{DQS}$ crossing	t_{WLS}	140	-	ps	
Write leveling hold time from rising DQS, $\overline{DQS}$ crossing to rising CK, $\overline{CK}$ crossing	t_{WLH}	140	-	ps	
Write leveling output delay	t_{WLO}	0	7.5	ns	
Write leveling output error	t_{WLOE}	0	2	ns	
Absolute clock period	t_{CK}(abs)	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	ps	
Absolute clock high pulse width	t_{CH}(abs)	0.43	-	t_{CK}(avg)	30
Absolute clock low pulse width	t_{CL}(abs)	0.43	-	t_{CK}(avg)	31
Clock period jitter	t_{JIT}(per)	-60	60	ps	
Clock period jitter during DLL locking period	t_{JIT}(per,lck)	-50	50	ps	
Cycle to cycle period jitter	t_{JIT}(cc)	-	120	ps	
Cycle to cycle period jitter during DLL locking period	t_{JIT}(cc,lck)	-	100	ps	
Cumulative error across 2 cycles	t_{ERR}(2per)	-88	88	ps	
Cumulative error across 3 cycles	t_{ERR}(3per)	-105	105	ps	
Cumulative error across 4 cycles	t_{ERR}(4per)	-117	117	ps	
Cumulative error across 5 cycles	t_{ERR}(5per)	-126	126	ps	
Cumulative error across 6 cycles	t_{ERR}(6per)	-133	133	ps	
Cumulative error across 7 cycles	t_{ERR}(7per)	-139	139	ps	

Parameter	Symbol	- 107 (DDR3-1866)		Unit	Note
		Min	Max		
Cumulative error across 8 cycles	t_{ERR}(8per)	-145	145	ps	
Cumulative error across 9 cycles	t_{ERR}(9per)	-150	150	ps	
Cumulative error across 10 cycles	t_{ERR}(10per)	-154	154	ps	
Cumulative error across 11 cycles	t_{ERR}(11per)	-158	158	ps	
Cumulative error across 12 cycles	t_{ERR}(12per)	-161	-161	ps	
Cumulative error across n = 13,14,...49,50 cycles	t_{ERR}(nper)	$t_{ERR}(nper)min = (1 + 0.68ln(n))*t_{JIT}(per)min$ $t_{ERR}(nper)max = (1 + 0.68ln(n))*t_{JIT}(per)max$		ps	32

Notes for AC Electrical Characteristics

NOTE :

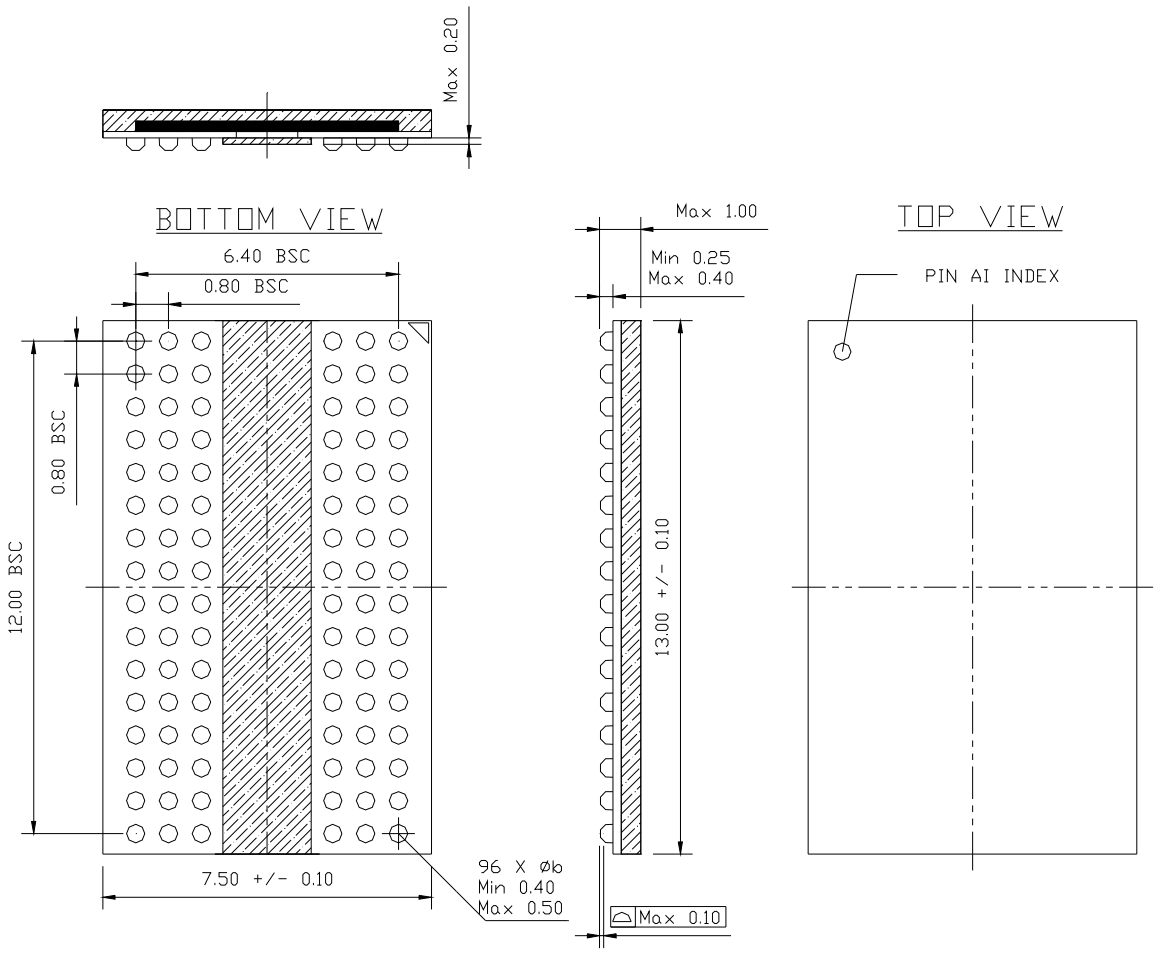
1. Actual value dependant upon measurement level definitions which are TBD.
2. Commands requiring a locked DLL are: READ (and READA) and synchronous ODT commands.
3. The max values are system dependent.
4. WR as programmed in mode register.
5. Value must be rounded-up to next higher integer value.
6. There is no maximum cycle time limit besides the need to satisfy the refresh interval, tREFI.
7. ODT turn on time (min) is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time (max) is when the ODT resistance is fully on. Both are measured from ODTLon.
8. ODT turn-off time (min) is when the device starts to turn-off ODT resistance. ODT turn-off time (max) is when the bus is in high impedance. Both are measured from ODTLoff.
9. tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR / tCK to the next integer.
10. WR in clock cycles as programmed in MR0.
11. The maximum read postamble is bound by tDQSCK(min) plus tQSH(min) on the left side and tHZ(DQS)max on the right side.
12. Output timing deratings are relative to the SDRAM input clock. When the device is operated with input clock jitter, this parameter needs to be derated by TBD.
13. Value is only valid for RON34.
14. Single ended signal parameter. Refer to the section of tLZ(DQS), tLZ(DQ), tHZ(DQS), tHZ(DQ) Notes for definition and measurement method.
15. tREFI depends on operating case temperature (Tc).
16. tIS(base) and tIH(base) values are for 1V/ns command/addresss single-ended slew rate and 2V/ns CK, $\overline{CK}$ differential slew rate, Note for DQ and DM signals, VREF(DC) = VREFDQ(DC). For input only pins except $\overline{RESET}$, VREF(DC) = VREFCA(DC). See Address / Command Setup, Hold and Derating section.
17. tDS(base) and tDH(base) values are for 1V/ns DQ single-ended slew rate and 2V/ns DQS, $\overline{DQS}$ differential slew rate. Note for DQ and DM signals,VREF(DC)= VREFDQ(DC). For input only pins except RESET, VREF(DC) = VREFCA(DC). See Data Setup, Hold and and Slew Rate Derating section.
18. Start of internal write transaction is defined as follows ;
    For BL8 (fixed by MRS and on-the-fly) : Rising clock edge 4 clock cycles after WL. For
    BC4 (on-the-fly) : Rising clock edge 4 clock cycles after WL.
    For BC4 (fixed by MRS) : Rising clock edge 2 clock cycles after WL.
19. The maximum read preamble is bound by tLZDQS(min) on the left side and tDQSCK(max) on the right side.
20. CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operation.
21. Although CKE is allowed to be registered LOW after a REFRESH command once tREFPDEN(min) is satisfied, there are cases where additional time such as tXPDLL(min) is also required.
22. Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.
23. One ZQCS command can effectively correct a minimum of 0.5 % (ZQCorrection) of RON and RTT impedance error within 64 nCK for all speed bins assuming the maximum sensitivities specified in the “Output Driver Voltage and Temperature Sensitivity” and “ODT Voltage and Temperature Sensitivity” tables. The appropriate interval between ZQCS commands can be determined from these tables and other application specific parameters.
    One method for calculating the interval between ZQCS commands, given the temperature (Tdriftrate) and voltage (Vdriftrate) drift rates that the SDRAM is subject to in the application, is illustrated. The interval could be defined by the following formula:

$$\frac{\text{ZQCorrection}}{(\text{TSens} \times \text{Tdriftrate}) + (\text{VSens} \times \text{Vdriftrate})}$$

    where TSens = max(dRTTdT, dRONdTM) and VSens = max(dRTTdV, dRONdVM) define the SDRAM temperature and voltage sensitivities.

24. The tIS(base) AC150 specifications are adjusted from the tIS(base) specification by adding an additional 100 ps of derating to accommodate for the lower alternate threshold of 150 mV and another 25 ps to account for the earlier reference point [(175 mv - 150 mV) / 1 V/ns].
25. Pulse width of a input signal is defined as the width between the first crossing of VREF(DC) and the consecutive crossing of VREF(DC).
26. tDQSL describes the instantaneous differential input low pulse width on DQS - $\overline{\text{DQS}}$, as measured from one falling edge to the next consecutive rising edge.
27. tDQSH describes the instantaneous differential input high pulse width on DQS - $\overline{\text{DQS}}$, as measured from one rising edge to the next consecutive falling edge.
28. tDQSH,act + tDQSL,act = 1 tCK,act ; with tXYZ,act being the actual measured value of the respective timing parameter in the application.
29. tDSH,act + tDSS,act = 1 tCK,act ; with tXYZ,act being the actual measured value of the respective timing parameter in the application.
30. tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.
31. tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.
32. n = from 13 cycles to 50 cycles. This row defines 38 parameters.

Package Diagram (x16)
96-Ball Fine Pitch Ball Grid Array Outline



NOTE: ALL DIMENSIONS ARE IN MILLIMETERS.

Revision History

Rev	History	Release Date	Remark
0.1	Initial release	May 2019	
1.0	Formal release Add DDR3-1866	Sep. 2019	