ECC DRAM

IME51(08/16)SDBET
512Mbit SDRAM with integrated ECC error correction
4 Bank x 16Mbit x 8
4 Bank x 8Mbit x 16

	6	75
System Frequency (f_{CK3}) $\overline{CAS}$ Latency = 3	166 MHz	133 MHz
System Frequency (f_{CK2}) $\overline{CAS}$ Latency = 2	100 MHz	100 MHz
Clock Cycle Time (t_{CK3}) $\overline{CAS}$ Latency = 3	6 ns	7.5 ns
Clock Cycle Time (t_{CK2}) $\overline{CAS}$ Latency = 2	10 ns	10 ns
Clock Access Time (t_{AC3}) $\overline{CAS}$ Latency = 3	5.4 ns	5.4 ns
Clock Access Time (t_{AC2}) $\overline{CAS}$ Latency = 2	6 ns	6 ns

Features

- High speed data transfer rates up to 166 MHz
- Full Synchronous Dynamic RAM, with all signals referenced to clock rising edge
- Single Pulsed $\overline{RAS}$ Interface
- Data Mask for Read/Write Control
- Four Banks controlled by BA0 & BA1
- Programmable $\overline{CAS}$ Latency: 2, 3
- Programmable Wrap Sequence: Sequential or Interleave
- Programmable Burst Length:
  1, 2, 4, 8 and full page for Sequential Type
  1, 2, 4, 8 for Interleave Type
- Multiple Burst Read with Single Write Operation
- Automatic and Controlled Precharge Command
- Random Column Address every CLK (1-N Rule)
- Power Down Mode
- Auto Refresh and Self Refresh
- Refresh Interval: 4096 cycles/64 ms
- Available in 54 Pin TSOP II
- LVTTL Interface
- Single +3.3 V ±0.3 V Power Supply
- Refresh cycles:
  - Average refresh period
    Commercial: 64 ms at 0°C ≤ Ta ≤ +70°C
    Industrial: 64 ms at -40°C ≤ Ta ≤ +85°C
    High Temperature: 64 ms at -40°C ≤ Ta ≤ +105°C
    X-Temp of Extreme Temperature:
    64 ms at -40°C ≤ Ta ≤ +125°C
    Y-Temp of Extreme Temperature:
    64 ms at Tc ≤ +105°C
    32 ms at Tc > +105°C
  * Min/Max temperature value depends on the temperature range of the specific device
- Operating temperature range
  - Commercial Ta = 0°C to +70°C
  - Industrial Ta = -40°C to +85°C
  - High Temperature
    Ta = -40°C to +105°C, Tc(max) = +115°C
  - X-Temp and Y-Temp of Extreme Temperature
    Ta = -40°C to +125°C, Tc(max) = +135°C

*Tc and Ta must not exceed the maximum operating temperature

Option — **Marking**

- Configuration
  - 64Mx8 (4 Bank x 16Mbit x 8) — 5108
  - 32Mx16 (4 Bank x 8Mbit x 16) — 5116
- Package
  - 54-pin TSOP — T
- Leaded/Lead-free
  - Leaded — <blank>
  - Lead-free/Rohs — G
- Speed/Cycle Time
  - 6ns @ CL3 (PC166) — -6
  - 7.5ns @ CL3 (PC133) — -75
- Temperature
  - Commercial 0°C to 70°C Ta — <blank>
  - Industrial -40°C to 85°C Ta — I
  - High -40°C to 105°C Ta (Tc max 115°C) — H
  - Extreme -40°C to 125°C Ta (Tc max 135°C) — X, Y
- Automotive Grade
  - Non-Automotive — <blank>
  - Automotive AEC-Q100 — A

  * Possible combinations: IA = AEC-Q100 Grade 3, HA = AEC-Q100 Grade 2, XA/YA = AEC-Q100 Grade 1

Example Part Number: IME5108SDBETG-75IA

Description

The IME51(08/16)SDBET is a four bank Synchronous DRAM organized as 4 banks x 16Mbit x 8 (5108), 4 banks x 8Mbit x 16 (5116).

The IME51(08/16)SDBET achieves high speed data transfer rates up to 166 MHz by employing a chip architecture that prefetches multiple bits and then synchronizes the output data to a system clock.

All of the control, address, data input and output circuits are synchronized with the positive edge of an externally supplied clock.

Operating the four memory banks in an interleaved fashion allows random access operation to occur at higher rate than is possible with standard DRAMs. A sequential and gapless data rate of up to 166 MHz is possible depending on burst length, $\overline{CAS}$ latency and speed grade of the device.

Special Features (ECC – Functionality)

- Embedded error correction code (ECC) functionality corrects single bit errors within each 64 bit memory-word.
- The error correction is performed automatically inside the ECC DRAM device.
- Parity data is generated by an internal ECC logic and then stored in additional, dedicated memory space
- Fully compatible to JEDEC standard DRAM operation and timings
- JEDEC compliant FBGA package (drop in replacement)

ECC – Functionality / Challenges and Achievements

During the production test, the ECC DRAMs are verified to pass extensive burn-in, core-function and speed tests throughout the complete memory array, including the memory-space for the parity-data. Only when every single memory cell has passed these tests, the ECC function is switched on by hardware and the products get shipped. With the ECC function activated, customers will have unparalleled functionality and quality.

Embedded ECC functionality

Intelligent Memory ECC DRAMs are JEDEC compliant components with integrated error-correction. The internal logic automatically detects and corrects single-bit-errors "on the fly" without any delays or additional latencies compared to conventional DRAM components. ECC DRAMs have additional memory-space to store the ECC-check-bits. Internally, the ECC DRAM works with a 72 bit wide buffer. When writing to the DRAM, an additional 8 ECC check-bits are being generated per each 64 bit data-word. Upon a Read-command, the whole 64+8 bit word is transferred to the buffer and automatically corrected by an ECC Hamming Code (72, 64). The corrected data is then applied to the DQ lines of the ECC DRAM in bit-widths of 4, 8, 16 or 32 bit, depending on the organization of the device.

The ECC algorithm is able to detect and correct one bit-error per 64+8 bit data-word. A 1 Gigabit ECC DRAM component has 16,777,216 data-words of 64 Bits. In each of these data-words, one single-bit error could be corrected, resulting in approximately 16 million times higher reliability of ECC DRAM compared to a conventional DRAM with similar capacity.

Note: If Burst Length x DRAM-I/O-width < 64 bit during a Write-command, the ECC-functionality is limited. Please contact Intelligent Memory for further details.

Comparison to conventional ECC implementation

ECC error correction is very common on high end industrial applications and servers. It normally requires an ECC-capable memory-controller which has an extra-wide data-bus with for example 72 bits (64 data-bits + 8 check-bits). The memory controller generates the required additional check-bits for the data and writes the extra wide data-word to the memory. Upon a Read-command, the memory controller will verify the data-integrity of the data-word + check-bits and performs the correction algorithm. Performing this algorithm affects the systems performance. In addition to the requirement for an ECC-capable memory controller, the conventional way of ECC correction requires multiple DRAMs to be accessed in parallel to achieve the extra-wide bit-width. On Server-memory-modules, for example, 18 DRAM-components with 4 data-lines each are put in parallel to reach the total 72 bit extra-wide data-bus.

With IM ECC DRAM, the check-bit-generation, verification and correction is performed inside the memory device. Every single ECC DRAM
performs the error correction by itself, thus it does not require ECC-capable processors/controllers nor any wide data-bus between the controller and the DRAM. Because the ECC DRAM components are JEDEC compliant, they are drop-in replacements to conventional DRAM-memory. Any existing application that is currently built with conventional DRAM can be equipped with error-correction functionality. Note that, if a standard 64 bit memory-module is built using ECC DRAMs, the depth of error-correction is deeper than on 72 bit ECC memory module as each DRAM component on the module performs its own ECC correction-algorithm.

Why is ECC error correction important?

Numerous analyzes and field-studies have proven DRAM single-bit errors to be the root cause of system-malfunctions or data-corruptions.
According to the field-study by the University Of Toronto called "DRAM Errors In The Wild – A Large-Scale field study", 25000 to 70000 ECC correctable single-bit errors occur per Megabit of DRAM within 1 billion hours of operation.
While not every single bit error causes a system crash, the application-software may become unstable or important data can be altered and the wrong data can pass through to external media, resulting in unrecoverable data-errors.

While all DRAMs are factory-tested by long burn-in-testing and effective functional and speed testing with different patterns and voltage variations, single-bit errors are technically not avoidable.
The effects are typically transient and difficult-to-repeat single data-bit flips. Many of these single-bit errors appear only under heavy stress or longer time of use of the DRAM, resulting as random system malfunctions or data-corruptions of the application. After a reset, the systems work again until the next occurrence of a single bit error reappears. It is difficult to prove a defect, as it is only a random effect which shows up in different ways at unknown times.

ECC corrects the output, but not the content of the Memory Array. For maximum stability we recommend to do periodical "scrubbing" (read and overwrite)

Possible root-causes for single-bit errors

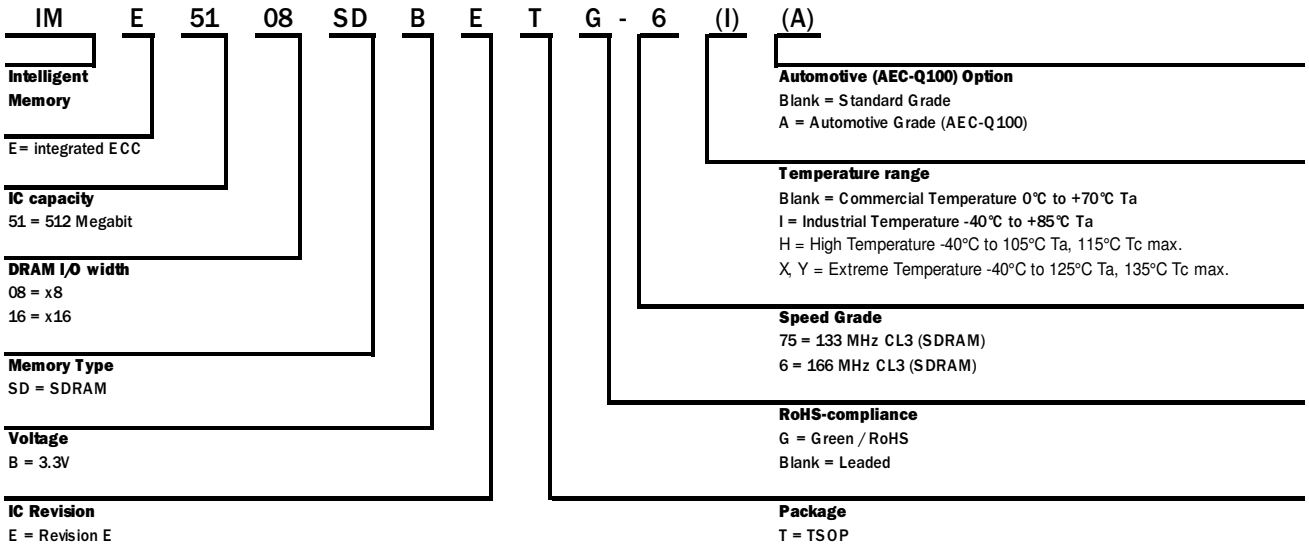
DRAM cells consist of capacitors holding an electric charge which defines if the memory-cell contains a logical 0 or a 1. These capacitor-cells are switched by transistors.
With the trend to smaller process technologies, higher speeds and lower supply-voltages, DRAM memory cells become more sensitive to noise on the signals, electromagnetic fields, cosmic rays or particle radiation. Also power peaks and variations in the signal-timing can cause single-bit errors.

Furthermore, depending on the age and intensity of use of those DRAM components, memory-cells suffer from various degrees of degradation. The isolation of the capacitors gets reduced and leakage increases, leading to lower data-retention-times of some cells. As data-retention times approach the refresh-times, data-bit tend to sometimes show up an incorrect binary value. The effects often appear only with certain data-patterns, at specific temperatures or at high data-traffic to the DRAM. The cell gets "weak", but the errors in the cell are not easily repeatable as they are not permanent.

There is no way to improve the DRAM technology itself, except by going back to larger processes, lower speeds and higher voltages. Pre-Testing the DRAMs longer, with more stress and wider guard bands, or even with automotive certified screening-processes does not fully protect from the risk of single-bit errors.

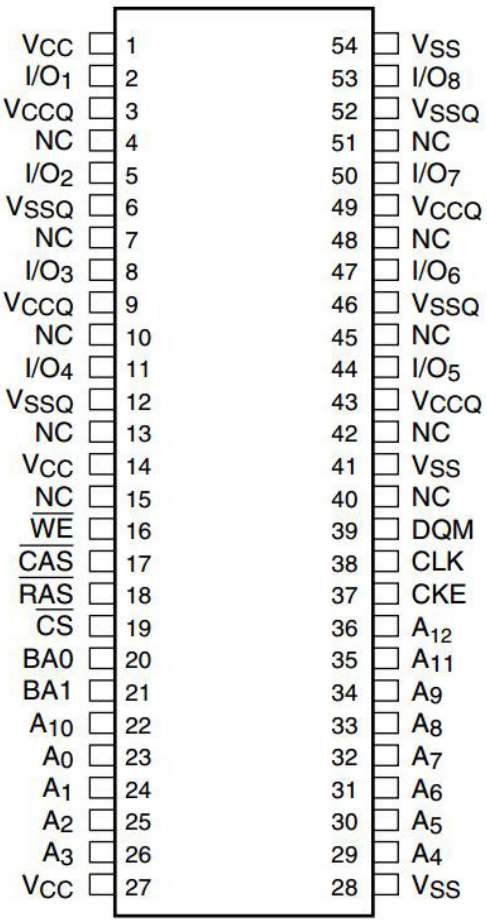
The only practical way to avoid single-bit errors is to use error correction algorithms such as ECC.

Part Number Information



Description	Pkg.	Pin Count
TSOP-II	T	54

54 Pin Plastic TSOP-II x8 PIN CONFIGURATION Top View

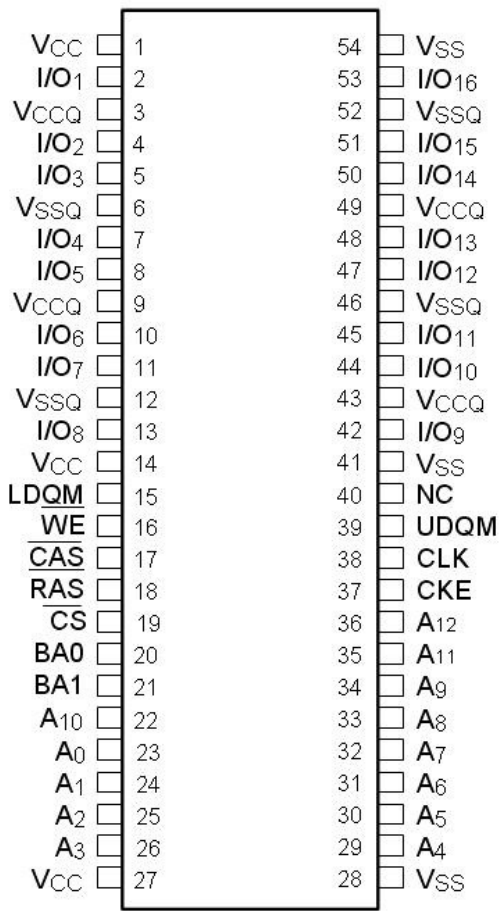


Pin Names

CLK	Clock Input
CKE	Clock Enable
$\overline{CS}$	Chip Select
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
A_0–A_{12}	Address Inputs
BA0, BA1	Bank Select
I/O_1–I/O_8	Data Input/Output
DQM	Data Mask
V_{CC}	Power (+3.0V~3.3V)
V_{SS}	Ground
V_{CCQ}	Power for I/O's (+3.0V~3.3V)
V_{SSQ}	Ground for I/O's
NC	Not connected

Description	Pkg.	Pin Count
TSOP-II	T	54

54 Pin Plastic TSOP-II x16 PIN CONFIGURATION Top View



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A_0–A_{12}	Address Inputs
BA0, BA1	Bank Select
I/O_1–I/O_{16}	Data Input/Output
LDQM, UDQM	Data Mask
V_{CC}	Power (+3.0V~3.3V)
V_{SS}	Ground
V_{CCQ}	Power for I/O's (+3.0V~3.3V)
V_{SSQ}	Ground for I/O's
NC	Not connected

Capacitance

(V_{CC} = V_{CCQ} = 3.3 V ± 0.3 V, f = 1 MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance: CLK	C_{I1}	2.5	3.5	pF
Input Capacitance: A0-A12, BA0, BA1, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$, CKE, DQM	C_{I2}	2.5	3.8	pF
Input/output Capacitance: DQ	C_{IO}	4.0	6.0	pF

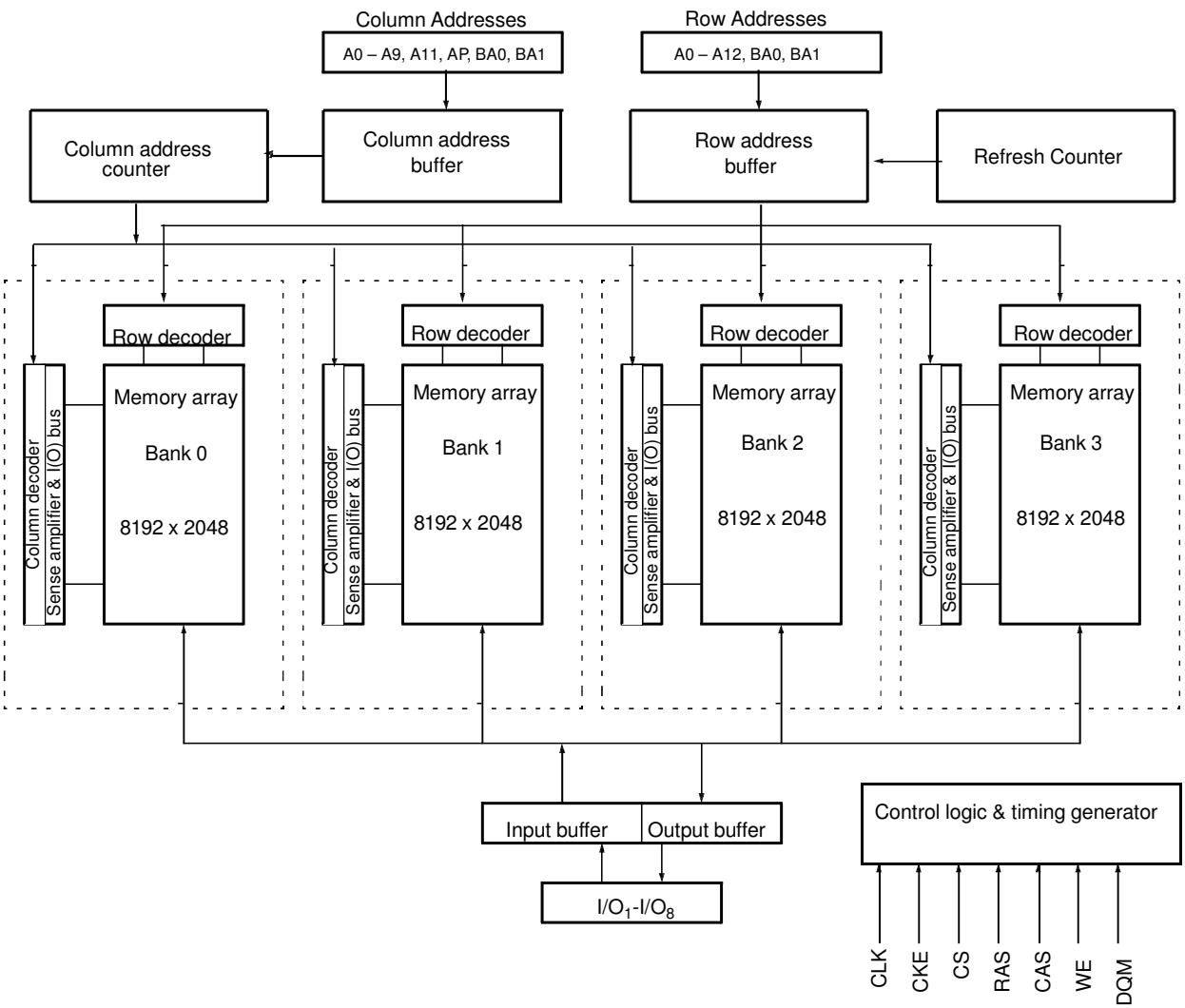
Absolute Maximum Ratings*

Operating temperature range .....0 to 70 °C for Commercial
-40 to 85 °C for Industrial
Ta: -40 to 105 °C, Tc(max): +115°C for High Temperature
Ta: -40 to 125 °C, Tc(max): +135°C for Extreme Temperature
Storage temperature range .....-55 to 150 °C
Input/output voltage ..... -1.0 to +4.6 V
Power supply voltage ..... -1.0 to +4.6 V
Power dissipation ..... 1 W
Data out current (short circuit) ..... 50 mA

***Note:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

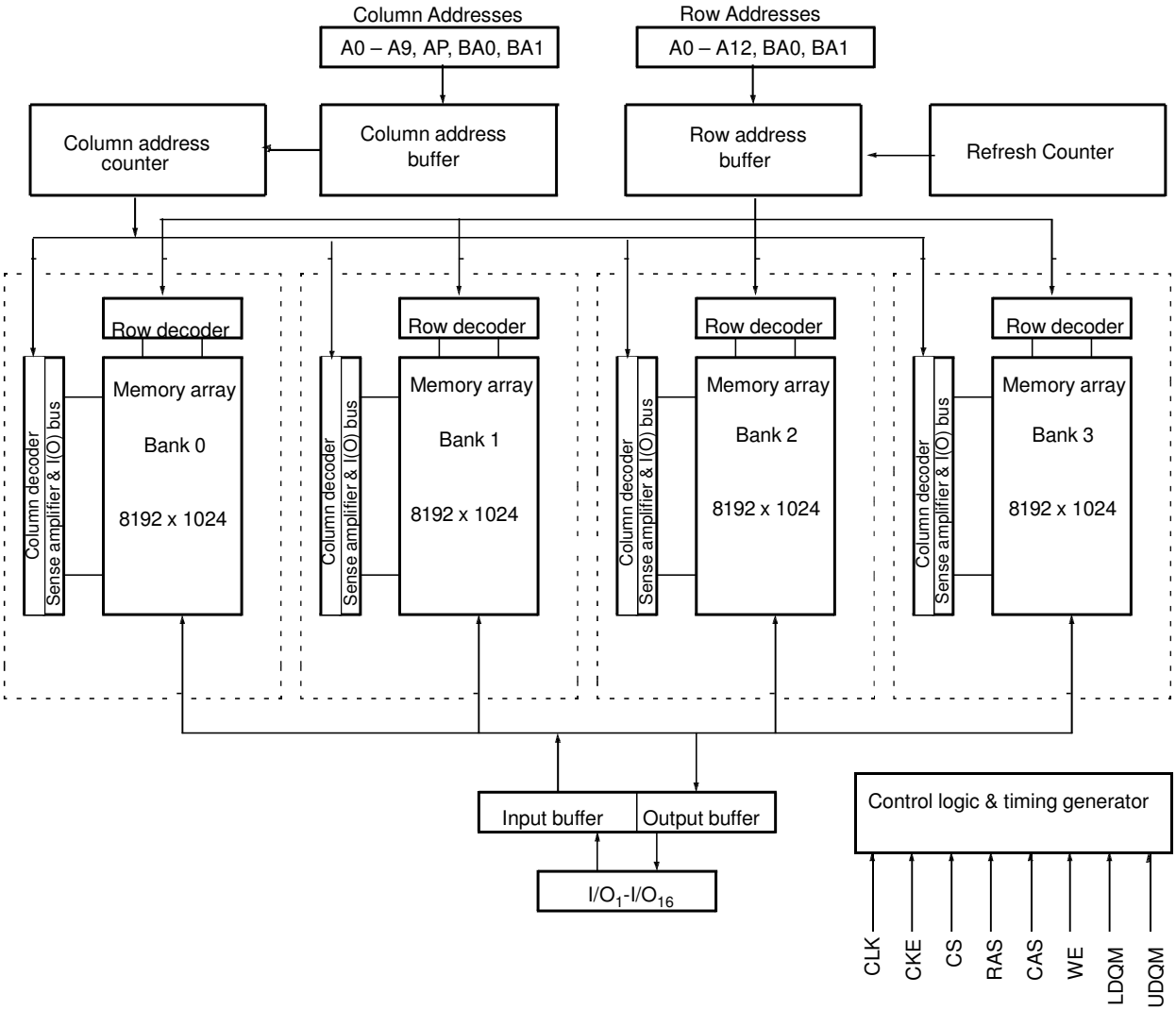
Block Diagram

X8 Configuration



Block Diagram

X16 Configuration



Signal Pin Description

Pin	Type	Signal	Polarity	Function
CLK	Input	Pulse	Positive Edge	The system clock input. All of the SDRAM inputs are sampled on the rising edge of the clock.
CKE	Input	Level	Active High	Activates the CLK signal when high and deactivates the CLK signal when low, thereby initiates either the Power Down mode or the Self Refresh mode.
$\overline{CS}$	Input	Pulse	Active Low	$\overline{CS}$ enables the command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.
$\overline{CAS}$, $\overline{RAS}$, $\overline{WE}$	Input	Pulse	Active Low	When sampled at the positive rising edge of the clock, $\overline{CAS}$, $\overline{RAS}$, and $\overline{WE}$ define the command to be executed by the SDRAM.
A0 - A12	Input	Level	—	During a Bank Activate command cycle, A0-A12 defines the row address (RA0-RA12) when sampled at the rising clock edge. During a Read or Write command cycle, A0-An defines the column address (CA0-CAn) when sampled at the rising clock edge. CAn depends from the SDRAM organization: • 64M x 8 SDRAM CA0–CA9, CA11. • 32M x 16 SDRAM CA0–CA9. In addition to the column address, A10(=AP) is used to invoke autoprecharge operation at the end of the burst read or write cycle. If A10 is high, autoprecharge is selected and BA0, BA1 defines the bank to be precharged. If A10 is low, autoprecharge is disabled. During a Precharge command cycle, A10(=AP) is used in conjunction with BA0 and BA1 to control which bank(s) to precharge. If A10 is high, all four banks will BA0 and BA1 are used to define which bank to precharge.
BA0, BA1	Input	Level	—	Selects which bank is to be active.
I/Ox	Input Output	Level	—	Data Input/Output pins operate in the same manner as on conventional DRAMs.
DQM LDQM UDQM	Input	Pulse	Active High	The Data Input/Output mask places the DQ buffers in a high impedance state when sampled high. In Read mode, DQM has a latency of two clock cycles and controls the output buffers like an output enable. In Write mode, DQM has a latency of zero and operates as a word mask by allowing input data to be written if it is low but blocks the write operation if DQM is high.
VCC, VSS	Supply	—	—	Power and ground for the input buffers and the core logic.
VCCQ VSSQ	Supply	—	—	Isolated power supply and ground for the output buffers to provide improved noise immunity.
NC	NC	—	—	Not Connected

Operation Definition

All of SDRAM operations are defined by states of control signals $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, and DQM at the positive edge of the clock. The following list shows the truth table for the operation commands.

Operation	Device State	CKE n-1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	A0-9, A11, A12	A10	BS0 BS1
Row Activate	Idle[3]	H	X	L	L	H	H	X	V	V	V
Read	Active[3]	H	X	L	H	L	H	X	V	L	V
Read w/Autoprecharge	Active[3]	H	X	L	H	L	H	X	V	H	V
Write	Active[3]	H	X	L	H	L	L	X	V	L	V
Write with Autoprecharge	Active[3]	H	X	L	H	L	L	X	V	H	V
Row Precharge	Any	H	X	L	L	H	L	X	X	L	V
Precharge All	Any	H	X	L	L	H	L	X	X	H	X
Mode Register Set	Idle	H	X	L	L	L	L	X	V	V	V
No Operation	Any	H	X	L	H	H	H	X	X	X	X
Device Deselect	Any	H	X	H	X	X	X	X	X	X	X
Auto Refresh	Idle	H	H	L	L	L	H	X	X	X	X
Self Refresh Entry	Idle	H	L	L	L	L	H	X	X	X	X
Self Refresh Exit	Idle (Self Refr.)	L	H	H	X	X	X	X	X	X	X
				L	H	H	X				
Power Down Entry	Idle Active[4]	H	L	H	X	X	X	X	X	X	X
				L	H	H	X				
Power Down Exit	Any (Power Down)	L	H	H	X	X	X	X	X	X	X
				L	H	H	L				
Data Write/Output Enable	Active	H	X	X	X	X	X	L	X	X	X
Data Write/Output Disable	Active	H	X	X	X	X	X	H	X	X	X

Notes:

1. V = Valid , x = Don't Care, L = Low Level, H = High Level
2. CKEn signal is input level when commands are provided, CKEn-1 signal is input level one clock before the commands are provided.
3. These are state of bank designated by BS0, BS1 signals.
4. Power Down Mode can not entry in the burst cycle.

Power On and Initialization

The default power on state of the mode register is supplier specific and may be undefined. The following power on and initialization sequence guarantees the device is preconditioned to each users specific needs. Like a conventional DRAM, the Synchronous DRAM must be powered up and initialized in a predefined manner. During power on, all VCC and VCCQ pins must be built up simultaneously to the specified voltage when the input signals are held in the “NOP” state. The power on voltage must not exceed VCC+0.3V on any of the input pins or VCC supplies. The CLK signal must be started at the same time. After power on, an initial pause of 200 us is required followed by a precharge of both banks using the precharge command. To prevent data contention on the DQ bus during power on, it is required that the DQM and CKE pins be held high during the initial pause period. Once all banks have been precharged, the Mode Register Set Command must be issued to initialize the Mode Register. A minimum of two Auto Refresh cycles (CBR) are also required.These may be done before or after programming the Mode Register. Failure to follow these steps may lead to unpredictable start-up modes.

Programming the Mode Register

The Mode register designates the operation mode at the read or write cycle. This register is divided into 4 fields. A Burst Length Field to set the length of the burst, an Addressing Selection bit to program the column access sequence in a burst cycle (interleaved or sequential), a CAS Latency Field to set the access time at clock cycle and a Operation mode field to differentiate between normal operation (Burst read and burst Write) and a special Burst Read and Single Write mode. The mode set operation must be done before any activate command after the initial power up. Any content of the mode register can be altered by re-executing the mode set command. All banks must be in precharged state and CKE must be high at least one clock before the mode set operation. After the mode register is set, a Standby or NOP command is required. Low signals of RAS, CAS, and $\overline{WE}$ at the positive edge of the clock activate the mode set operation. Address input data at this timing defines parameters to be set as shown in the previous table.

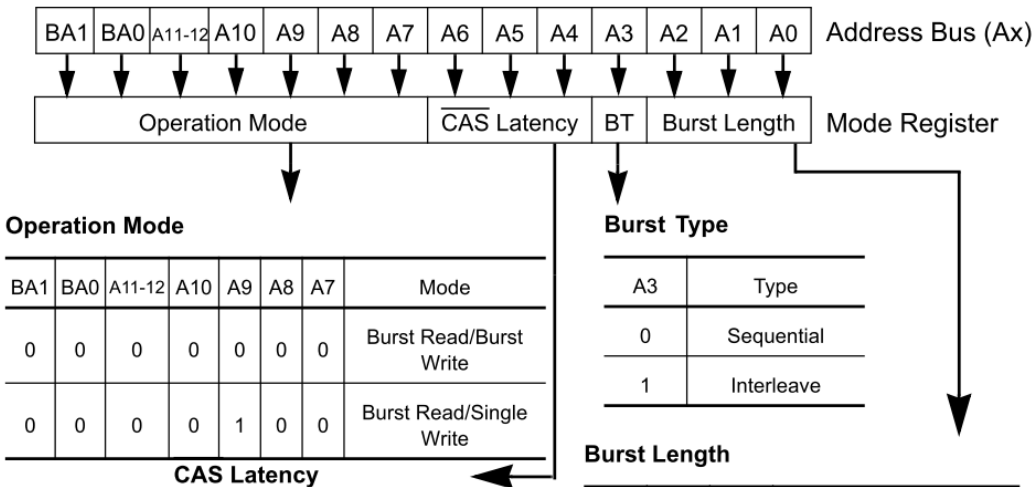
Read and Write Operation

When $\overline{RAS}$ is low and both $\overline{CAS}$ and $\overline{WE}$ are high at the positive edge of the clock, a RAS cycle starts. According to address data, a word line of the selected bank is activated and all of sense amplifiers associated to the wordline are set. A $\overline{CAS}$ cycle is triggered by setting $\overline{RAS}$ high and $\overline{CAS}$ low at a clock timing after a necessary delay, t_{RCD}, from the $\overline{RAS}$ timing. WE is used to define either a read ($\overline{WE}$ = H) or a write ($\overline{WE}$ = L) at this stage.

SDRAM provides a wide variety of fast access modes. In a single CAS cycle, serial data read or write operations are allowed at up to a 166 MHz data rate. The numbers of serial data bits are the burst length programmed at the mode set operation, i.e., one of 1, 2, 4, 8 and full page. Column addresses are segmented by the burst length and serial data accesses are done within this boundary. The first column address to be accessed is supplied at the CAS timing and the subsequent addresses are generated automatically by the programmed burst length and its sequence. For example, in a burst length of 8 with interleave sequence, if the first address is ‘2’, then the rest of the burst sequence is 3, 0, 1, 6, 7, 4, and 5.

Full page burst operation is only possible using sequential burst type. Full Page burst operation does not terminate once the burst length has been reached. (At the end of the page, it will wrap to the start address and continue.) In other words, unlike burst length of 2, 4, and 8, full page burst continues until it is terminated using another command.

Address Input for Mode Set (Mode Register Operation)



Operation Mode

BA1	BA0	A11-12	A10	A9	A8	A7	Mode
0	0	0	0	0	0	0	Burst Read/Burst Write
0	0	0	0	1	0	0	Burst Read/Single Write

CAS Latency

A6	A5	A4	Latency
0	0	0	Reserve
0	0	1	Reserve
0	1	0	2
0	1	1	3
1	0	0	Reserve
1	0	1	Reserve
1	1	0	Reserve
1	1	1	Reserve

Burst Type

A3	Type
0	Sequential
1	Interleave

Burst Length

A2	A1	A0	Length	
			Sequential	Interleave
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserve	Reserve
1	0	1	Reserve	Reserve
1	1	0	Reserve	Reserve
1	1	1	Full Page	Reserve

Similar to the page mode of conventional DRAM's, burst read or write accesses on any column address are possible once the RAS cycle latches the sense amplifiers. The maximum t_{RAS} or the refresh interval time limits the number of random column accesses. A new burst access can be done even before the previous burst ends. The interrupt operation at every clock cycles is supported. When the previous burst is interrupted, the remaining addresses are overridden by the new address with the full burst length. An interrupt which accompanies with an operation change from a read to a write is possible by exploiting DQM to avoid bus contention.

When two or more banks are activated sequentially, interleaved bank read or write operations are possible. With the programmed burst length, alternate access and precharge operations on two or more banks can realize fast serial data access modes among many different pages. Once two or more banks are activated, column to column interleave operation can be done between different pages.

Burst Length and Sequence:

Burst Length	Starting Address (A2 A1 A0)	Sequential Burst Addressing (decimal)	Interleave Burst Addressing (decimal)
2	xx0	0, 1	0, 1
	xx1	1, 0	1, 0
4	x00	0, 1, 2, 3	0, 1, 2, 3
	x01	1, 2, 3, 0	1, 0, 3, 2
	x10	2, 3, 0, 1	2, 3, 0, 1
	x11	3, 0, 1, 2	3, 2, 1, 0
8	000	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7
	001	1 2 3 4 5 6 7 0	1 0 3 2 5 4 7 6
	010	2 3 4 5 6 7 0 1	2 3 0 1 6 7 4 5
	011	3 4 5 6 7 0 1 2	3 2 1 0 7 6 5 4
	100	4 5 6 7 0 1 2 3	4 5 6 7 0 1 2 3
	101	5 6 7 0 1 2 3 4	5 4 7 6 1 0 3 2
	110	6 7 0 1 2 3 4 5	6 7 4 5 2 3 0 1
	111	7 0 1 2 3 4 5 6	7 6 5 4 3 2 1 0
Full Page	nnn	Cn, Cn+1, Cn+2....	not supported

Refresh Mode

SDRAM has two refresh modes, Auto Refresh and Self Refresh. Auto Refresh is similar to the $\overline{CAS}$ -before-$\overline{RAS}$ refresh of conventional DRAMs. All of banks must be precharged before applying any refresh mode. An on-chip address counter increments the word and the bank addresses and no bank information is required for both refresh modes.

The chip enters the Auto Refresh mode, when $\overline{RAS}$ and $\overline{CAS}$ are held low and CKE and $\overline{WE}$ are held high at a clock timing. The mode restores word line after the refresh and no external precharge command is necessary. A minimum tRC time is required between two automatic refreshes in a burst refresh mode. The same rule applies to any access command after the automatic refresh operation.

The chip has an on-chip timer and the Self Refresh mode is available. It enters the mode when $\overline{RAS}$, $\overline{CAS}$, and CKE are low and $\overline{WE}$ is high at a clock timing. All of external control signals including the clock are disabled. Returning CKE to high enables the clock and initiates the refresh exit operation. After the exit command, at least one t_{RC} delay is required prior to any access command.

DQM Function

DQM has two functions for data I/O read and write operations. During reads, when it turns to “high” at a clock timing, data outputs are disabled and become high impedance after two clock delay (DQM Data Disable Latency t_{DQZ}). It also provides a data mask function for writes. When DQM is activated, the write operation at the next clock is prohibited (DQM Write Mask Latency t_{DQW} = zero clocks).

Power Down

In order to reduce standby power consumption, a power down mode is available. All banks must be precharged and the necessary Precharge delay (t_{RP}) must occur before the SDRAM can enter the Power Down mode. Once the Power Down mode is initiated by holding CKE low, all of the receiver circuits except CLK and CKE are gated off. The Power Down mode does not perform any refresh operations, therefore the device can’t remain in Power Down mode longer than the Refresh period (t_{REF}) of the device. Exit from this mode is performed by taking CKE “high”. One clock delay is required for mode entry and exit.

Auto Precharge

Two methods are available to precharge SDRAMs. In an automatic precharge mode, the CAS timing accepts one extra address, CA10, to determine whether the chip restores or not after the operation. If CA10 is high when a Read Command is issued, the **Read with Auto-Precharge** function is initiated. The SDRAM automatically enters the precharge operation one clock before the last data out for $\overline{CAS}$ latencies 2, two clocks for $\overline{CAS}$ latencies 3 and three clocks for CAS latencies 4. If CA10 is high when a Write Command is issued, the **Write with Auto-Precharge** function is initiated. The SDRAM automatically enters the precharge operation a time delay equal to t_{WR} (Write recovery time) after the last data in. **Auto-Precharge** does not apply to full-page burst mode.

Precharge Command

There is also a separate precharge command available. When $\overline{RAS}$ and $\overline{WE}$ are low and $\overline{CAS}$ is high at a clock timing, it triggers the precharge operation. Three address bits, BA0, BA1 and A10 are used to define banks as shown in the following list. The precharge command can be imposed one clock before the last data out for CAS latency = 2, two clocks before the last data out for CAS latency = 3. Writes require a time delay twr from the last data out to apply the precharge command. A full-page burst may be truncated with a Precharge command to the same bank.

Bank Selection by Address Bits:

A10	BA0	BA1	
0	0	0	Bank 0
0	0	1	Bank 1
0	1	0	Bank 2
0	1	1	Bank 3
1	X	X	all Banks

Burst Termination

Once a burst read or write operation has been initiated, there are several methods in which to terminate the burst operation prematurely. These methods include using another Read or Write Command to interrupt an existing burst operation, use a Precharge Command to interrupt a burst cycle and close the active bank, or using the Burst Stop Command to terminate the existing burst operation but leave the bank open for future Read or Write Commands to the same page of the active bank. When interrupting a burst with another Read or Write Command care must be taken to avoid I/O contention. The Burst Stop Command, however, has the fewest restrictions making it the easiest method to use when terminating a burst operation before it has been completed. If a Burst Stop command is issued during a burst write operation, then any residual data from the burst write cycle will be ignored. Data that is presented on the I/O pins before the Burst Stop Command is registered will be written to the memory. The full-page burst is used in conjunction with Burst Terminate Command to generate arbitrary burst lengths.

DC Characteristics

Parameter	Symbol	Limit Values		Unit	Notes
		Min	Max		
Input high voltage	V_{IH}	2.0	V_{CCQ}+0.3	V	1, 2
Input low voltage	V_{IL}	- 0.3	+0.8	V	1, 2
Output high voltage (I_{OUT} = – 4.0 mA)	V_{OH}	2.4	–	V	1
Output low voltage (I_{OUT} = 4.0 mA)	V_{OL}	–	0.4	V	1
Input leakage current, any input (0 V < V_{IN} < V_{CC}, all other inputs = 0 V)	$I_{I(L)}$	- 10	+10	uA	
Output leakage current (DQ is disabled, 0 V < V_{OUT} < V_{CC})	$I_{O(L)}$	- 10	+10	uA	

Note:

1. All voltages are referenced to V_{SS}.
2. V_{IH} may overshoot to V_{CC} + 2.0 V for pulse width of < 4ns with 3.3V. V_{IL} may undershoot to -2.0 V for pulse width < 4.0 ns with 3.3V. Pulse width measured at 50% points with amplitude measured peak to DC reference.

Operating Currents

V_{CC} = 3.3 V ± 0.3 V (Recommended Operating Conditions unless otherwise noted)

Symbol	Parameter & Test Condition		Speed Grade	Max			Note
				X16	X8		
IDD1	Operating Current t_{RC} = $t_{RCMIN.}$, t_{RC} = t_{CKMIN}. Active-precharge command cycling, without Burst Operation	1 bank operation	-6	80	80	mA	1, 3
			-75	60	60		
IDD2P	Precharge Standby Current in Power Down Mode $\overline{CS}$ =V_{IH}, CKE≤ $V_{IL(max)}$	t_{CK} = min.	-6	4	4	mA	1, 3
			-75	4	4		
IDD2N	Precharge Standby Current in Non Power Down Mode $\overline{CS}$ =V_{IH}, CKE≥ $V_{IL(max)}$	t_{CK} = min.	-6	15	15	mA	3
			-75	15	15		
IDD3P	$\overline{CS}$ = $V_{IH(min)}$, CKE≤ $V_{IL(max)}$	t_{CK} = min.	-6	6	6	mA	3
			-75	6	6		
IDD3N	$\overline{CS}$ = $V_{IH(min)}$, CKE≥ $V_{IH(min)}$	t_{CK} = min.	-6	20	20	mA	3
			-75	20	20	mA	3
IDD4	Burst Operating Current Read/Write command cycling	t_{CK} = min.	-6	100	90	mA	1,2,3
			-75	80	70		
IDD5	t_{RC} = t_{RCMIN}	t_{CK} = min.	-6	170	170	mA	1,3
			-75	170	170		
IDD6	Self Refresh Current Self Refresh Mode, CKE≤ 0.2V		-6	5	5	mA	3
			-75	5	5		

Notes:

1. These parameters depend on the cycle rate and these values are measured by the cycle rate under the minimum value of t_{CK} and t_{RC}. Input signals are changed one time during t_{CK}.
2. These parameter depend on output loading. Specified values are obtained with output open.
3 The temperature from -55°C ~ 125°C

AC Characteristics [1,2,3]

V_{SS} = 0 V; V_{CC} = 3.3 V ± 0.3 V, t_T = 1 ns

#	Symbol	Parameter	Limit Values				Unit	
			-6		-75			
			Min	Max	Min	Max		
1	t_{CK}	Clock Cycle Time $\overline{CAS}$ Latency = 3 $\overline{CAS}$ Latency = 2	 6 10	 – –	 7.5 10	 – –	ns	
2	t_{CK}	Clock Frequency $\overline{CAS}$ Latency = 3 $\overline{CAS}$ Latency = 2	 – –	 166 100	 – –	 133 100	MHz	
3	t_{AC}	Access Time from Clock $\overline{CAS}$ Latency = 3 $\overline{CAS}$ Latency = 2	 – –	 5.4 6.0	 – –	 5.4 6.0	ns	2, 3
4	tCH	CLK HIGH Level Width	2.5	-	2.5	-	ns	
5	tCL	CLK LOW Level Width	2.5	-	2.5	-	ns	
6	tOH	Output Data Hold Time	2.7	-	2.7	-	ns	2
7	tLZ	Output LOW Impedance Time	1	-	1	-	ns	
8	tHZ3	Output HIGH Impedance Time	-	5.4	-	5.4	ns	
9	tHZ2		-	6	-	6	ns	
10	tDS	Input Data Setup Time	1.5	-	1.5	-	ns	
11	tDH	Input Data Hold Time	0.8	-	0.8	-	ns	
12	tAS	Address Setup Time	1.5	-	1.5	-	ns	
13	tAH	Address Hold Time	0.8	-	0.8	-	ns	
14	tCKS	CKE Setup Time	1.5	-	1.5	-	ns	
15	tCKH	CKE Hold Time	0.8	-	0.8	-	ns	
16	tCMS	Command Setup Time (CS, RAS, CAS, WE, DQM)	1.5	-	1.5	-	ns	
17	tCMH	Command Hold Time (CS, RAS, CAS, WE, DQM)	0.8	-	0.8	-	ns	
18	tRC	Command Period (REF to REF/ACT to ACT)	60	-	66	-	ns	5
19	tRAS	Command Period (ACT to PRE)	42	100K	44	120K	ns	5
20	tRP	Command Period (PRE to ACT)	15	-	15	-	ns	5
21	tRCD	Active Command To Read/Write Command Delay Time	18	-	15	-	ns	
22	tRRD	Command Period (ACT [0] to ACT[1])	12	-	15	-	ns	5
23	tWR	Last Data Input to Precharge (Write without Auto Precharge)	12	-	15	-	ns	
24	tDAL	Last Data Input to Precharge (Write with Auto Precharge)	30	-	30	-	ns	
25	tMRD	Mode Register Set-up to Command delay	2	-	2	-	tCK	
26	tDDE	Power Down Exit Setup Time	6	-	7.5	-	ns	

27	tSREX	Self-Refresh Exit Time	70	-	75	-	ns	
28	tT	Transition Time	0.3	1.2	0.3	1.2	ns	
29	tREF	Refresh Cycle Time Commercial Ta = 0°C to +70°C Industrial Ta = -40°C to +85°C High Temperature Ta = -40°C to +105°C, Tc(max) = +115°C X-Temp of Extreme Temp. Ta = -40°C to +125°C, Tc(max) = +135°C Y-Temp of Extreme Temp. Tc = -40°C to +105°C	-	64	-	64	ms	
		Refresh Cycle Time Y-Temp of Extreme Temperature Tc > +105°C, Tc(max) = +135°C	-	32	-	32	ms	

Notes for AC Parameters:

2. For proper power-up see the operation section of this data sheet.
2. AC timing tests have V_{IL} = 0.4V and V_{IH} = 2.4V with the timing referenced to the 1.4 V crossover point. The transition time is measured between V_{IH} and V_{IL}. All AC measurements assume t_T = 1ns with the AC output load circuit shown in Figure 1.

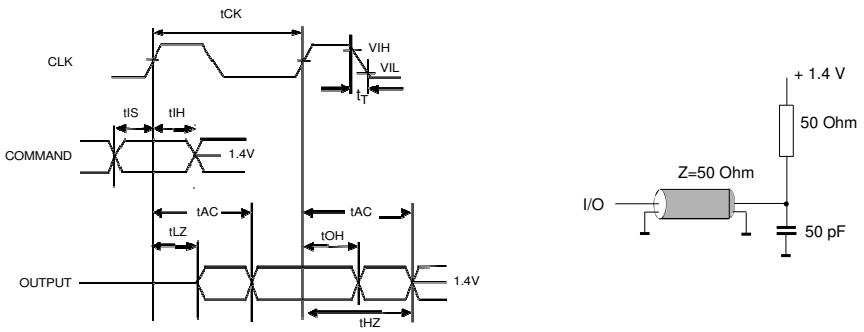


Figure 1.

3. If clock rising time is longer than 1 ns, a time (t_T/2 – 0.5) ns has to be added to this parameter.
4. If t_T is longer than 1 ns, a time (t_T – 1) ns has to be added to this parameter.
5. These parameter account for the number of clock cycle and depend on the operating frequency of the clock, as follows:

   the number of clock cycle = specified value of timing period (counted in fractions as a whole number)

   Self Refresh Exit is a synchronous operation and begins on the 2nd positive clock edge after CKE returns high. Self Refresh Exit is not complete until a time period equal to tRC is satisfied once the Self Refresh Exit command is registered.

6. Referenced to the time which the output achieves the open circuit condition, not to output voltage levels.

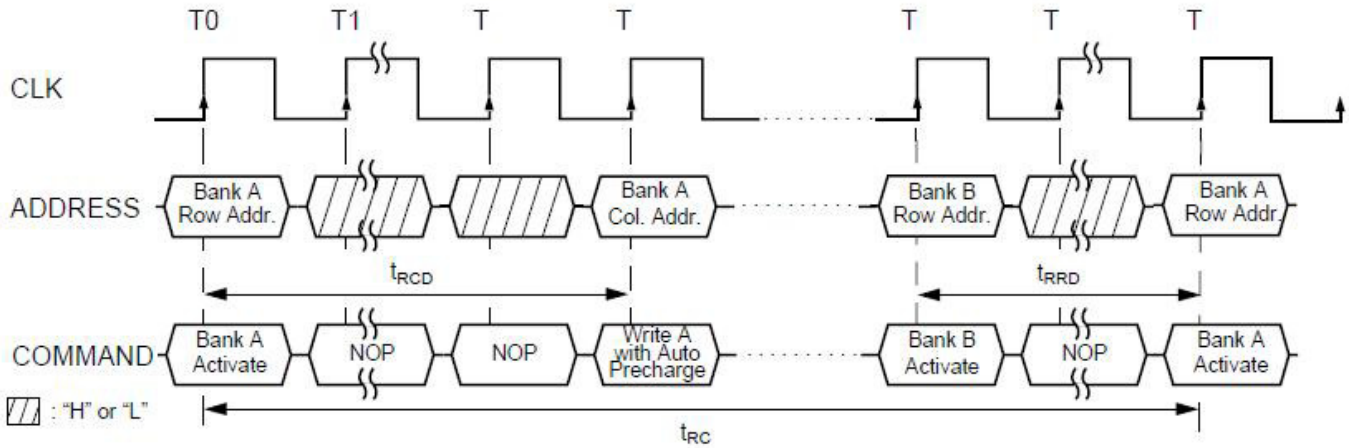
Timing Diagrams

Timing Diagrams (Cont'd)

15. Random Column Read (Page within same Bank)
    - 15.1 $\overline{CAS}$ Latency = 2
    - 15.2 $\overline{CAS}$ Latency = 3
16. Random Column Write (Page within same Bank)
    - 16.1 $\overline{CAS}$ Latency = 2
    - 16.2 $\overline{CAS}$ Latency = 3
17. Random Row Read (Interleaving Banks) with Precharge
    - 17.1 $\overline{CAS}$ Latency = 2
    - 17.2 $\overline{CAS}$ Latency = 3
18. Random Row Write (Interleaving Banks) with Precharge
    - 18.1 $\overline{CAS}$ Latency = 2
    - 18.2 $\overline{CAS}$ Latency = 3
19. Precharge Termination of a Burst
    - 19.1 $\overline{CAS}$ Latency = 2
    - 19.2 $\overline{CAS}$ Latency = 3
20. Full Page Burst Operation
    - 20.1 Full Page Burst Read, $\overline{CAS}$ Latency = 2
    - 20.2 Full Page Burst Read, $\overline{CAS}$ Latency = 3
21. Full Page Burst Operation
    - 21.1 Full Page Burst Write, $\overline{CAS}$ Latency = 2
    - 21.2 Full Page Burst Write, $\overline{CAS}$ Latency = 3

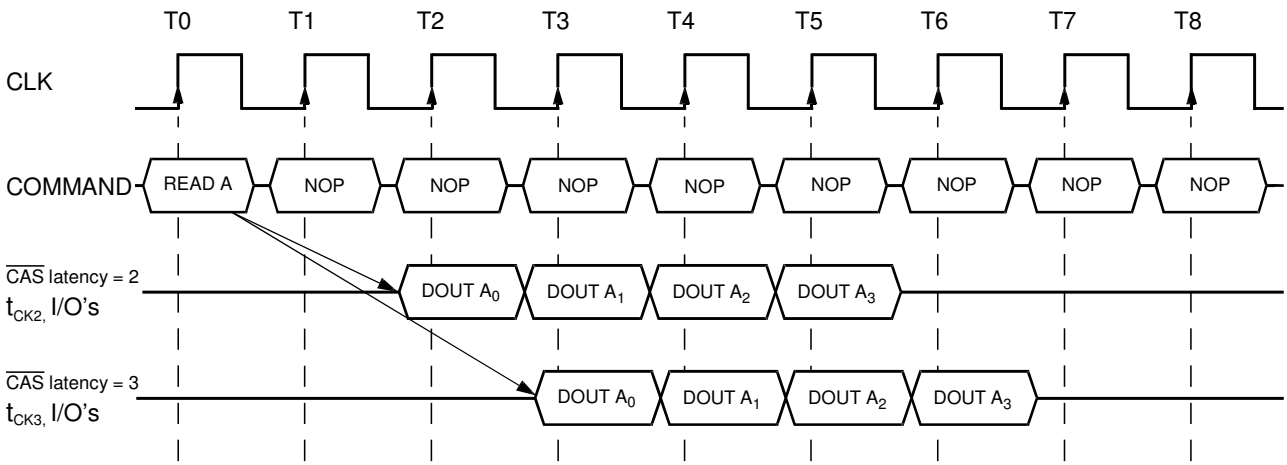
1. Bank Activate Command Cycle

($\overline{CAS}$ latency = 3)



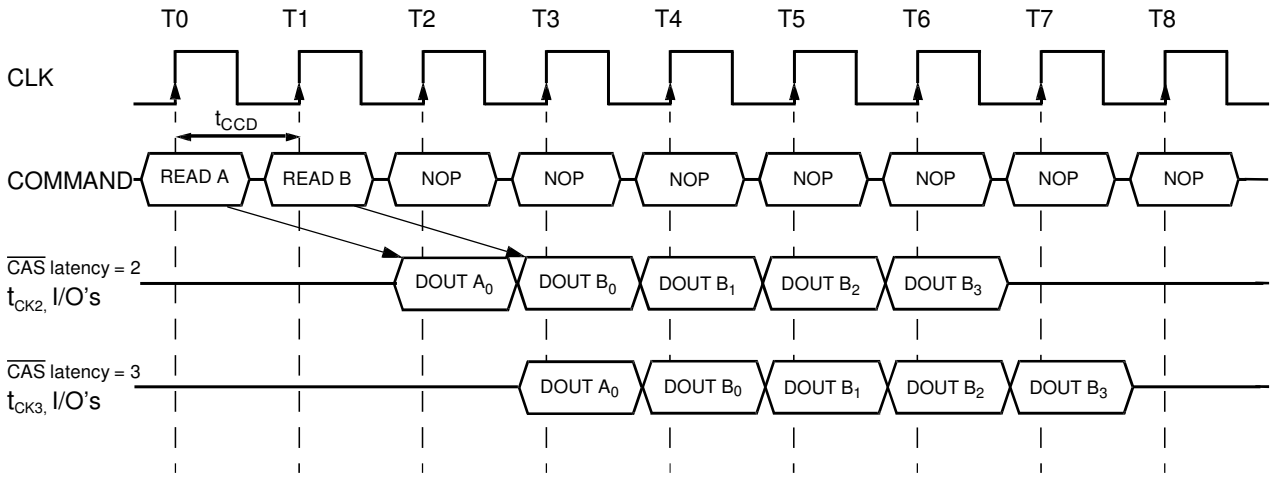
2. Burst Read Operation

(Burst Length = 4, $\overline{CAS}$ latency = 2, 3)



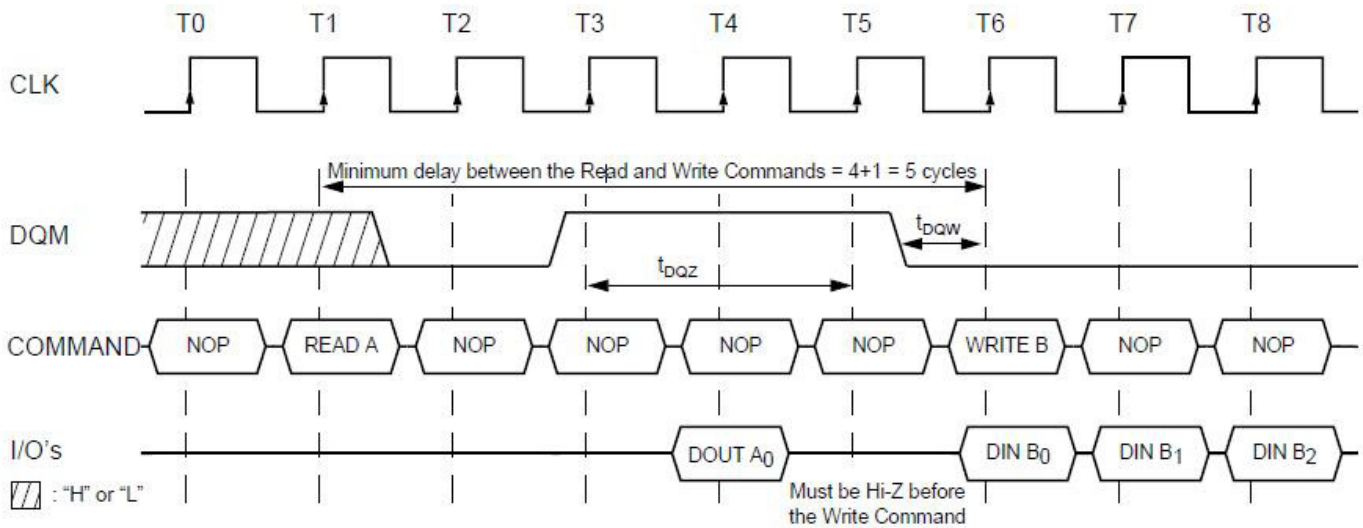
3. Read Interrupted by a Read

(Burst Length = 4, $\overline{CAS}$ latency = 2, 3)



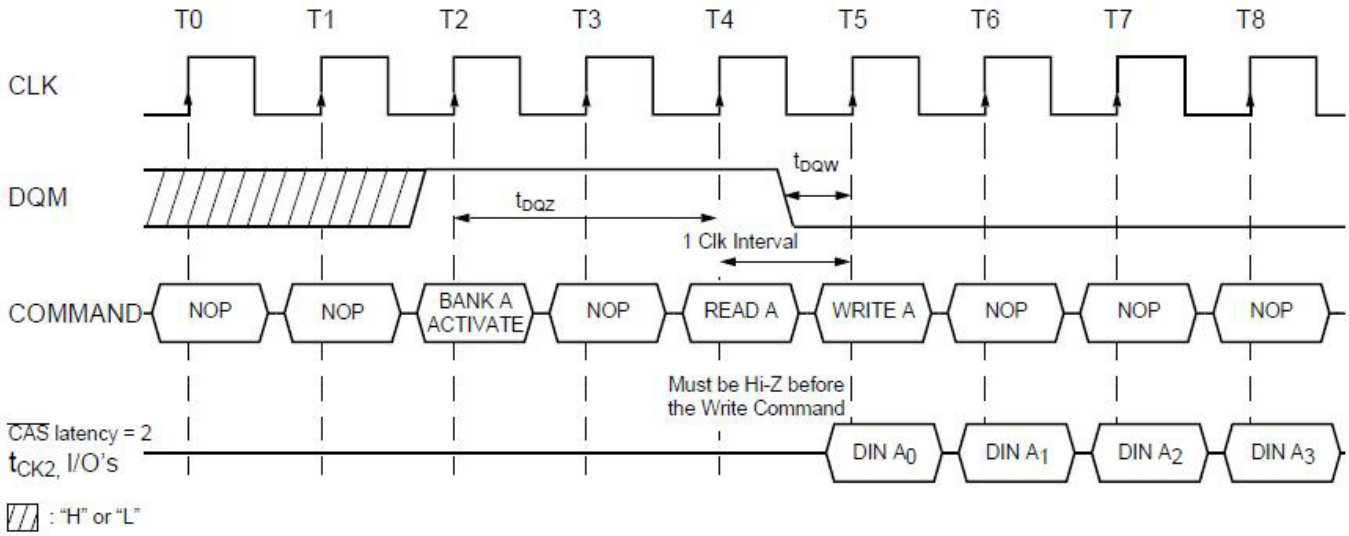
4.1 Read to Write Interval

(Burst Length = 4, $\overline{CAS}$ latency = 3)



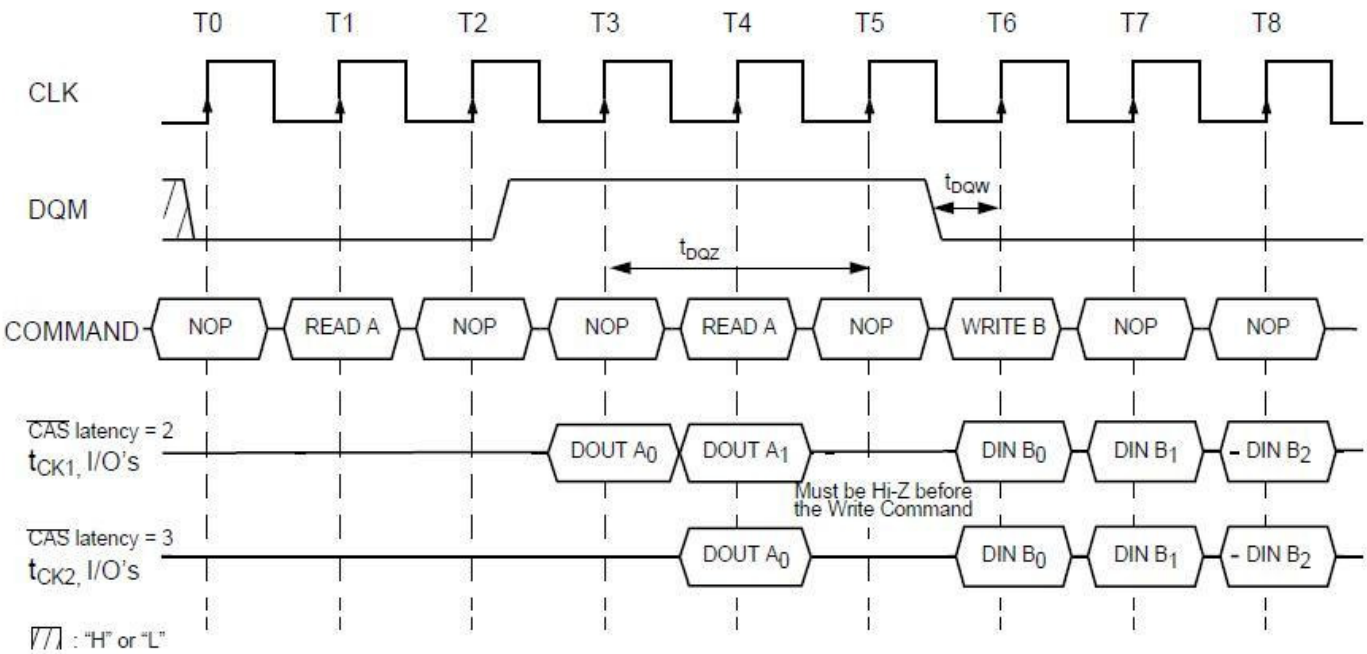
4.2 Minimum Read to Write Interval

(Burst Length = 4, $\overline{CAS}$ latency = 2)



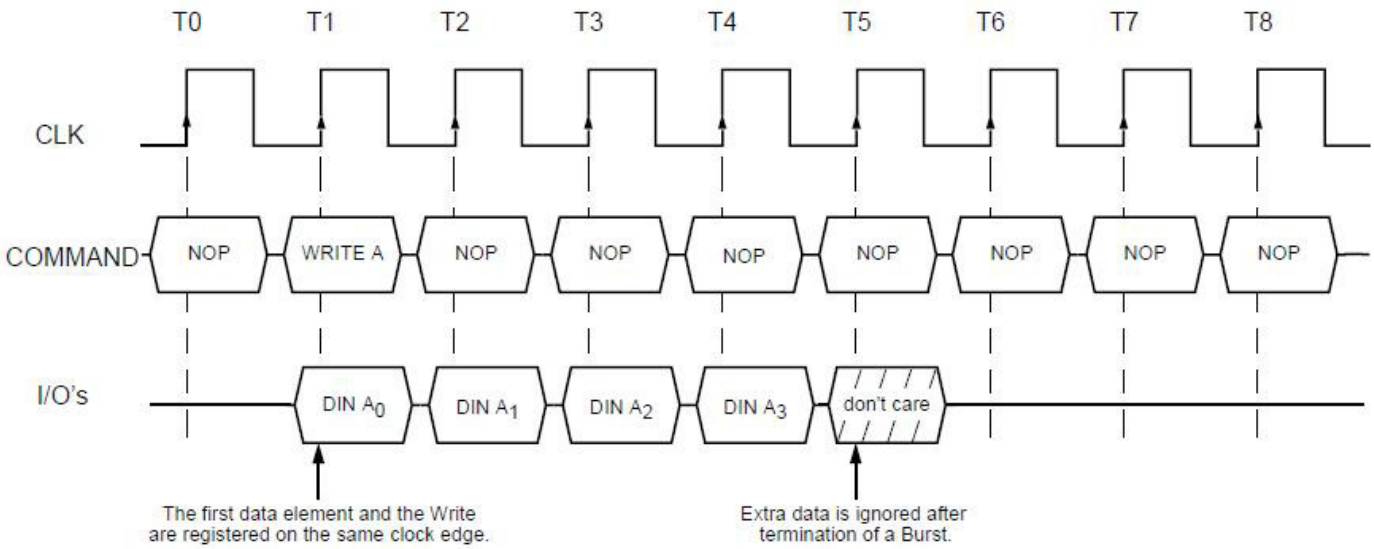
4.3 Non-Minimum Read to Write Interval

(Burst Length = 4, $\overline{CAS}$ latency = 2, 3)



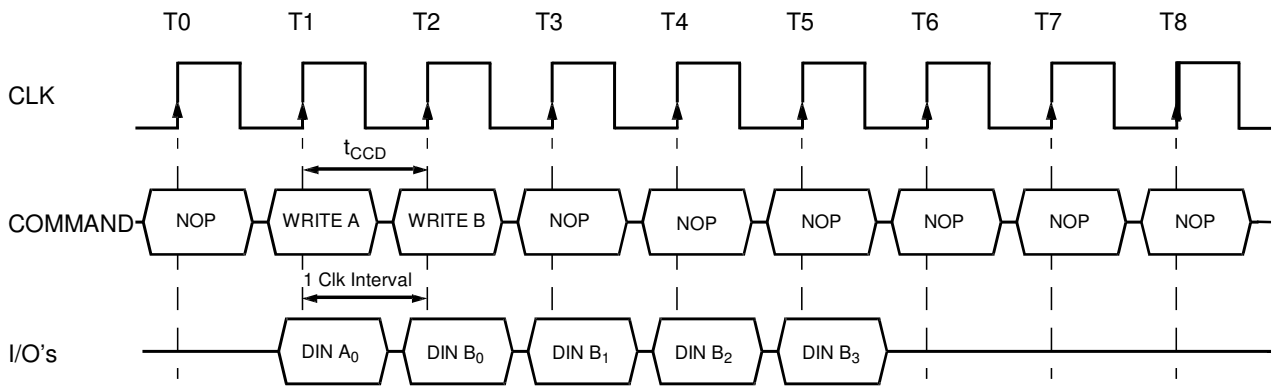
5. Burst Write Operation

(Burst Length = 4, $\overline{CAS}$ latency = 2, 3)



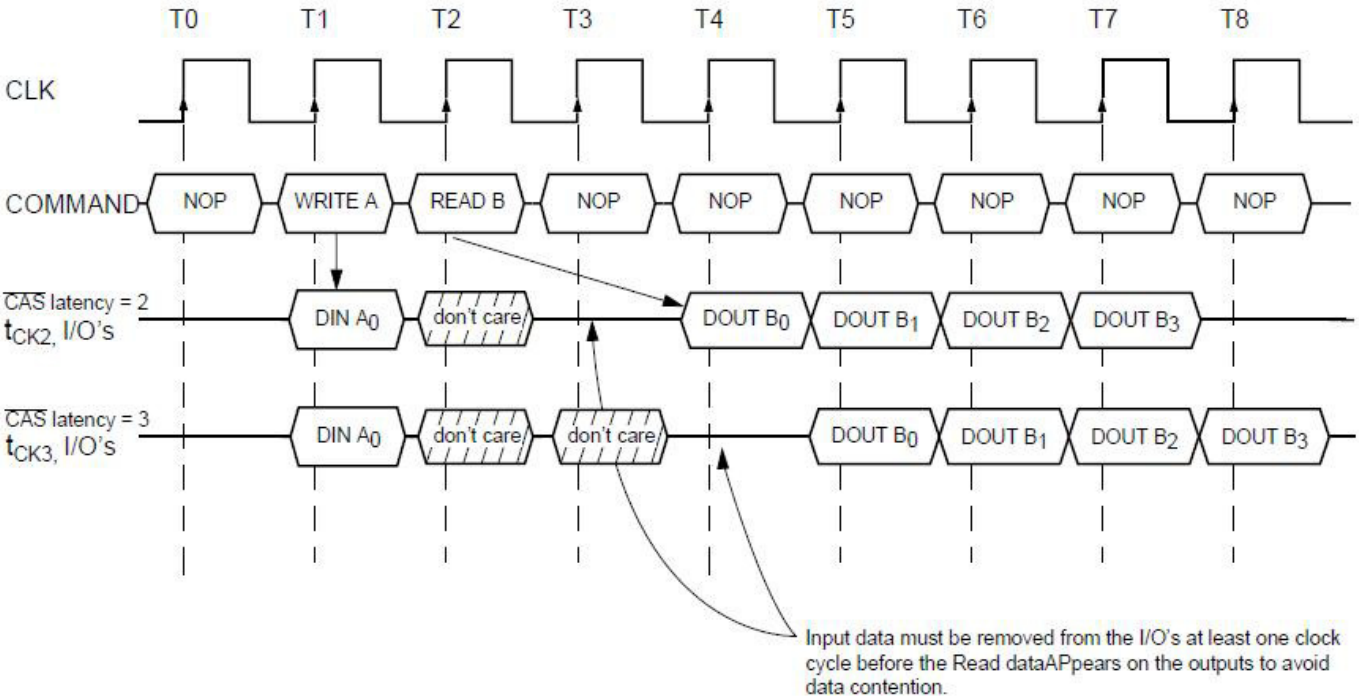
6.1 Write Interrupted by a Write

(Burst Length = 4, $\overline{CAS}$ latency = 2, 3)



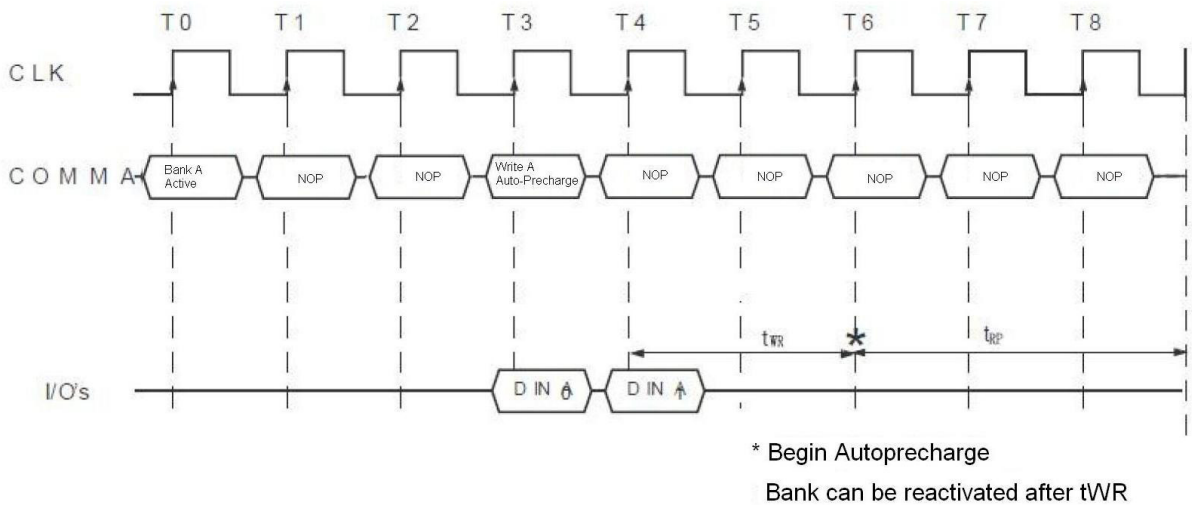
6.2 Write Interrupted by a Read

(Burst Length = 4, $\overline{CAS}$ latency = 2, 3)



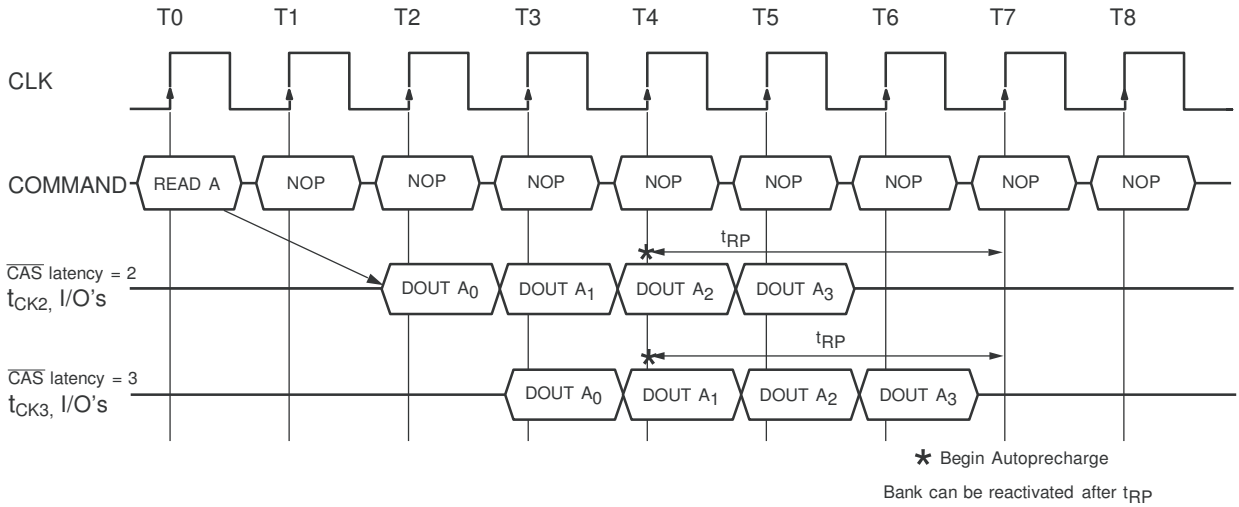
7.1 Burst Write with Auto-Precharge

Burst Length = 2, $\overline{CAS}$ latency = 2, 3)



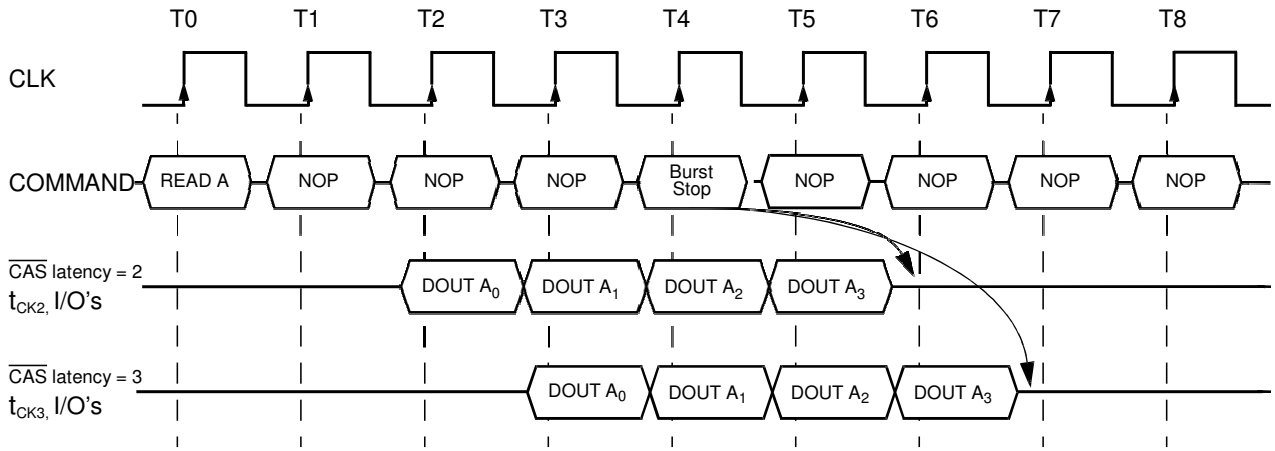
7.2 Burst Read with Auto-Precharge

Burst Length = 4, $\overline{\text{CAS}}$ latency = 2, 3)



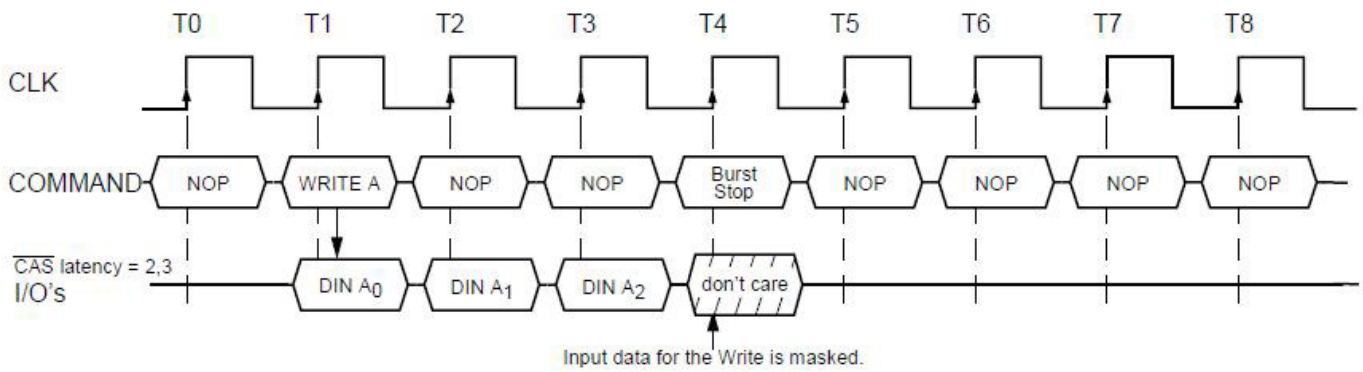
8.1 Termination of a Burst Read Operation

(CAS latency = 2, 3)

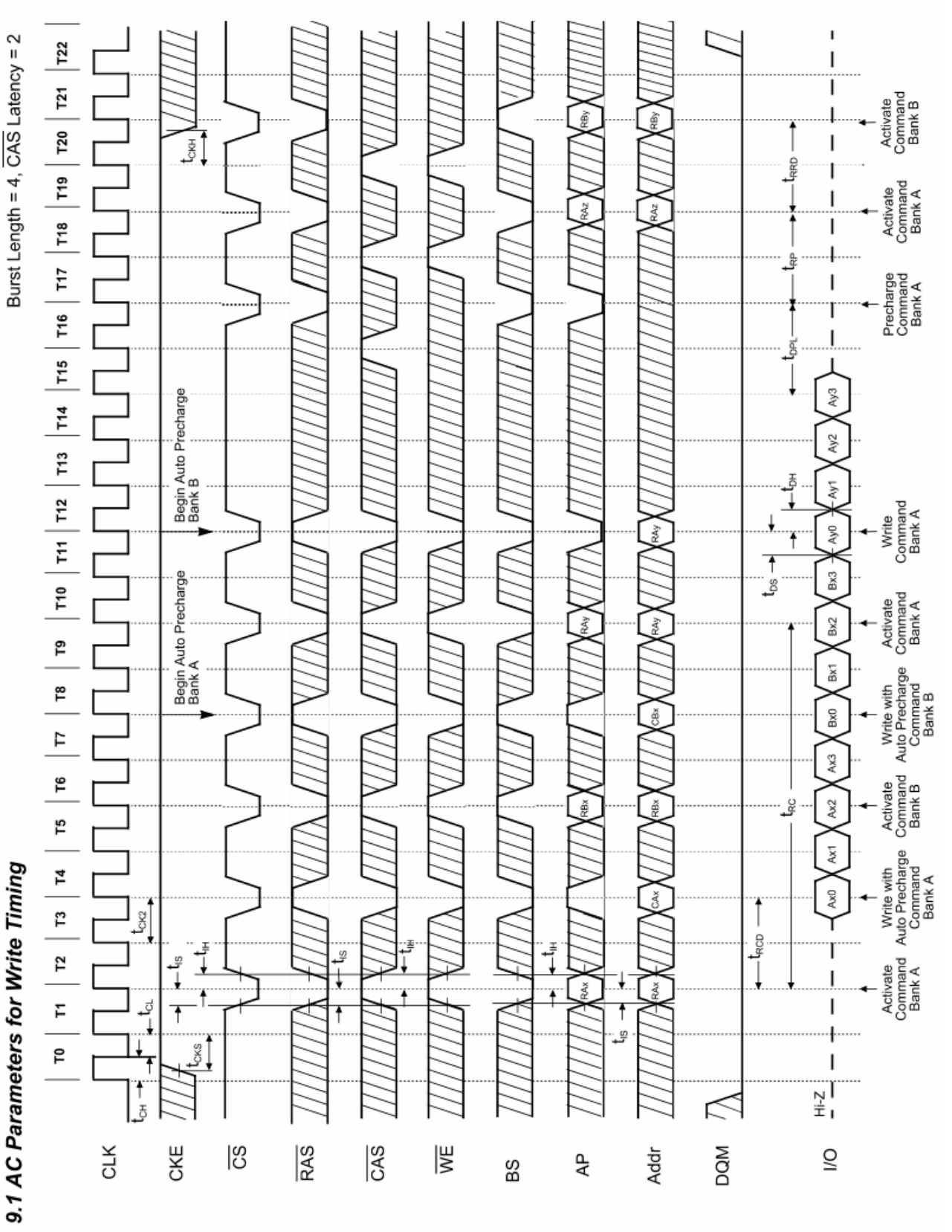


8.2 Termination of a Burst Write Operation

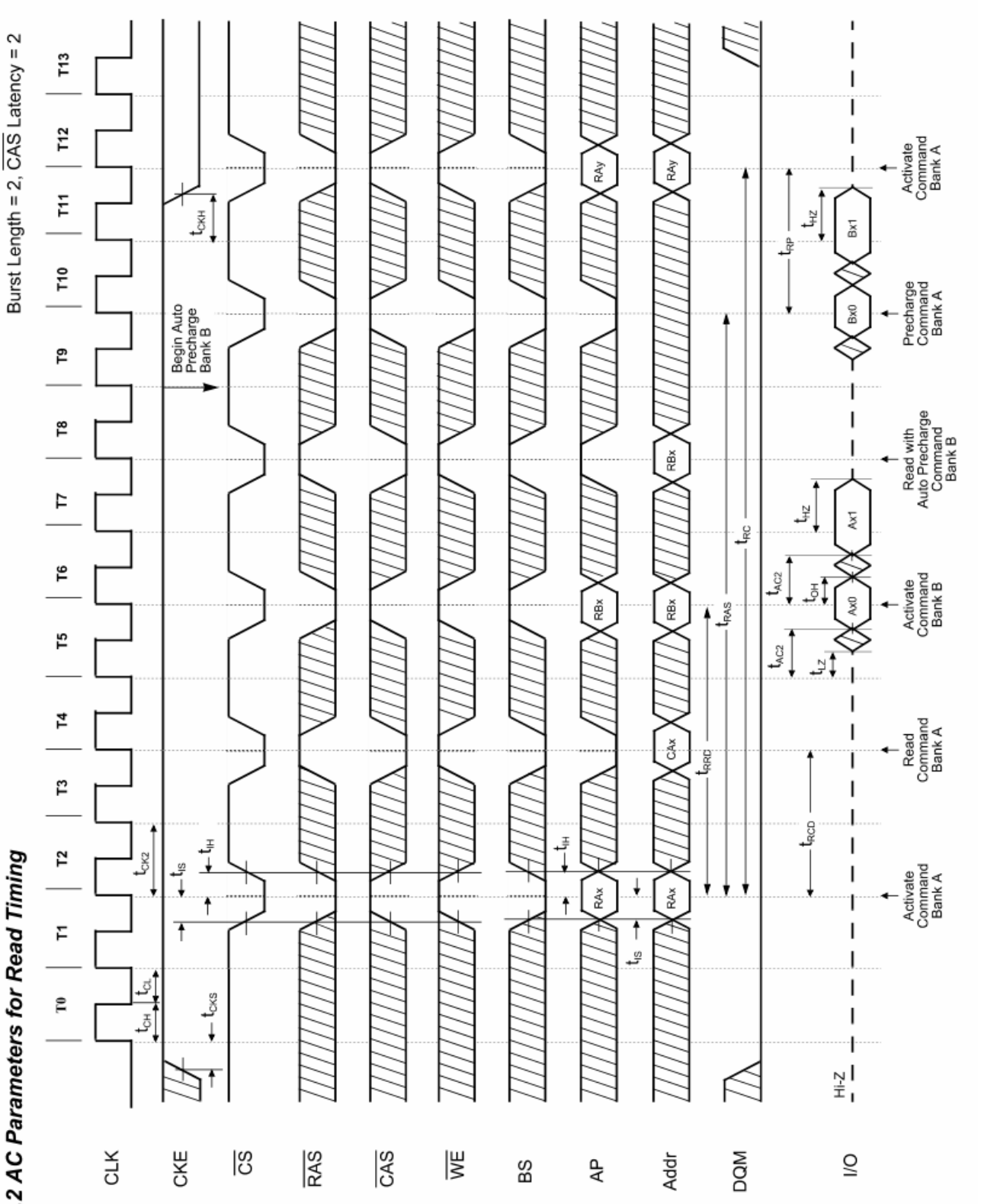
(CAS latency = 2, 3)



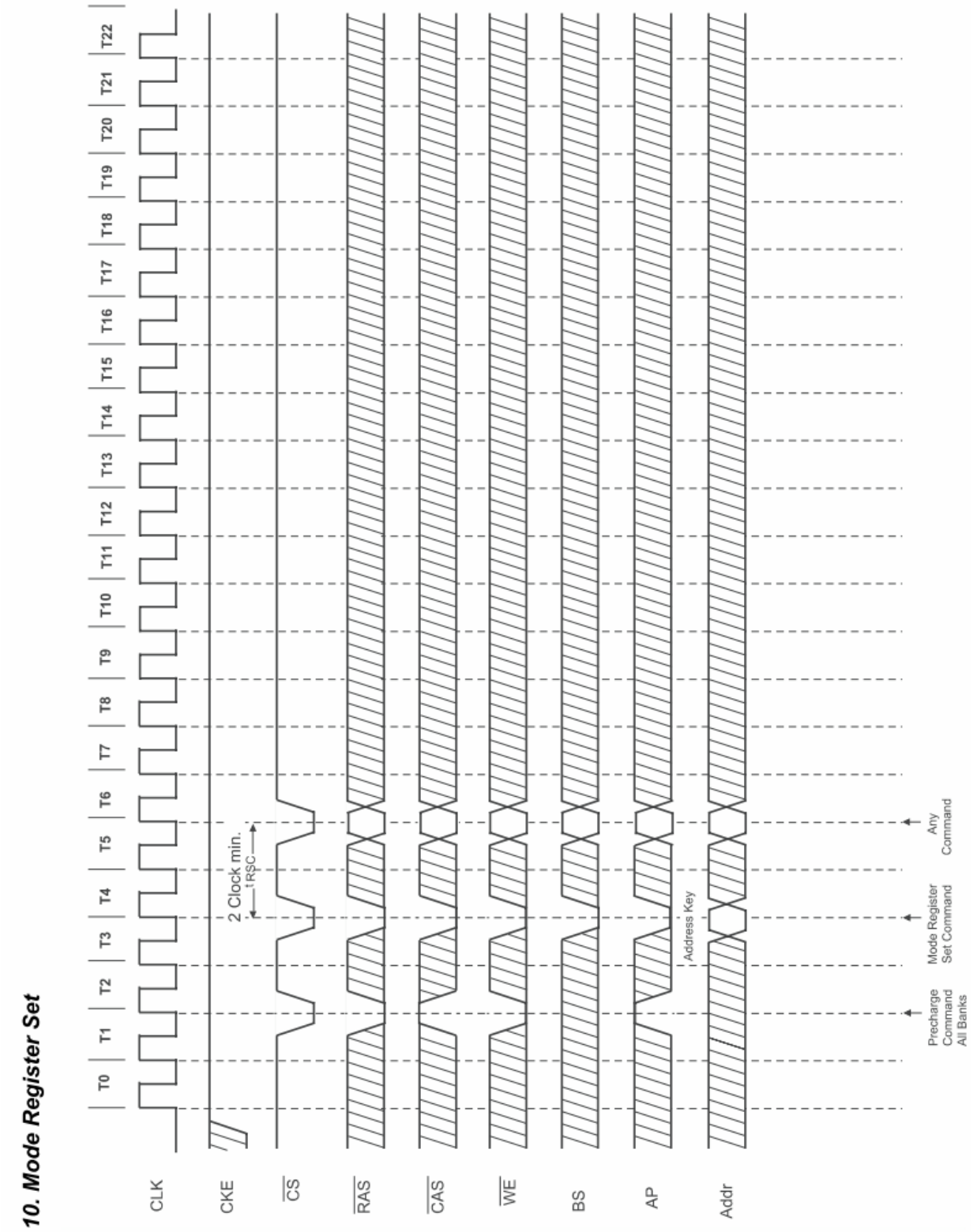
9.1 AC Parameters for Write Timing



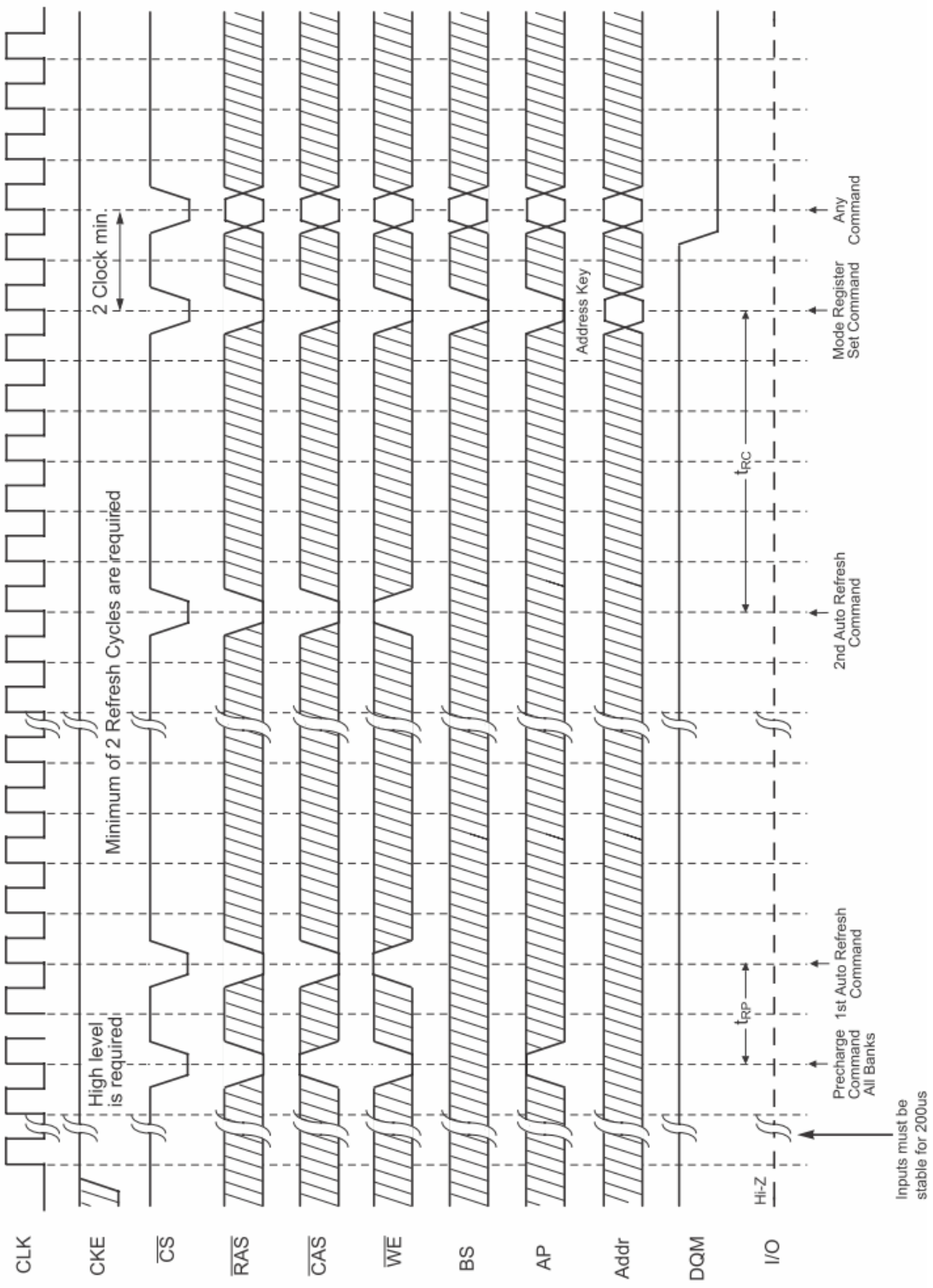
9.2 AC Parameters for Read Timing



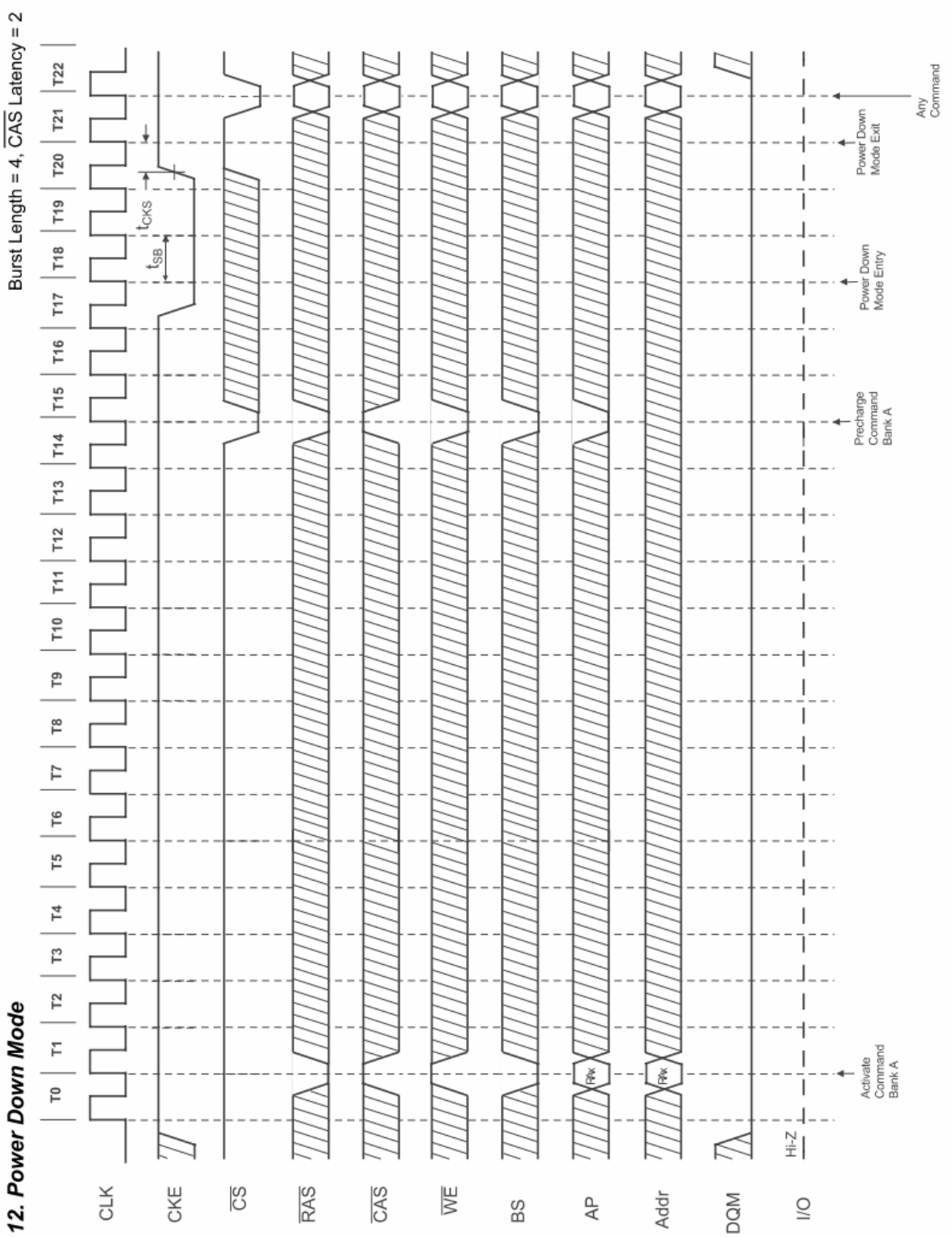
10. Mode Register Set



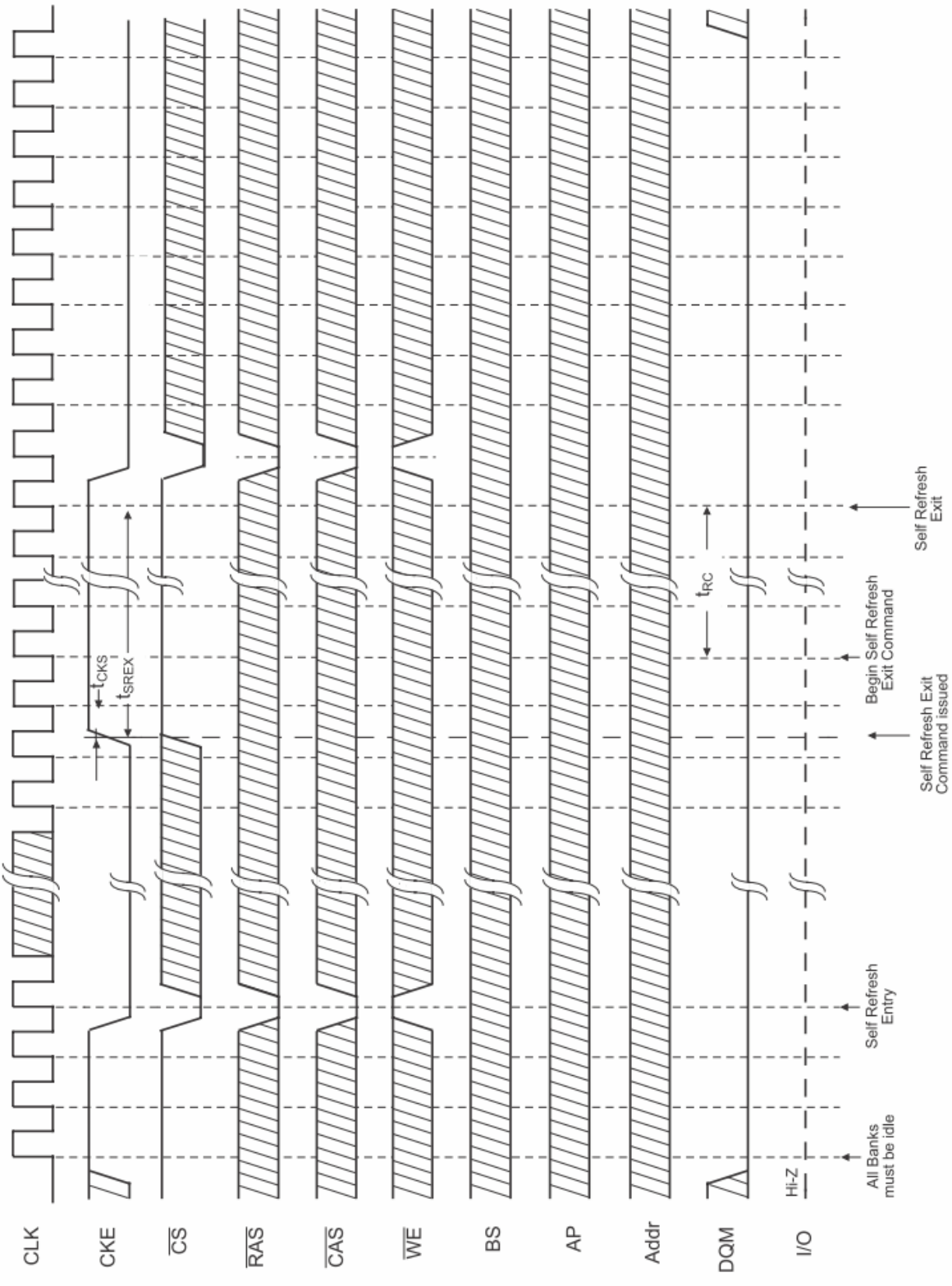
11. Power on Sequence and Auto Refresh (CBR)



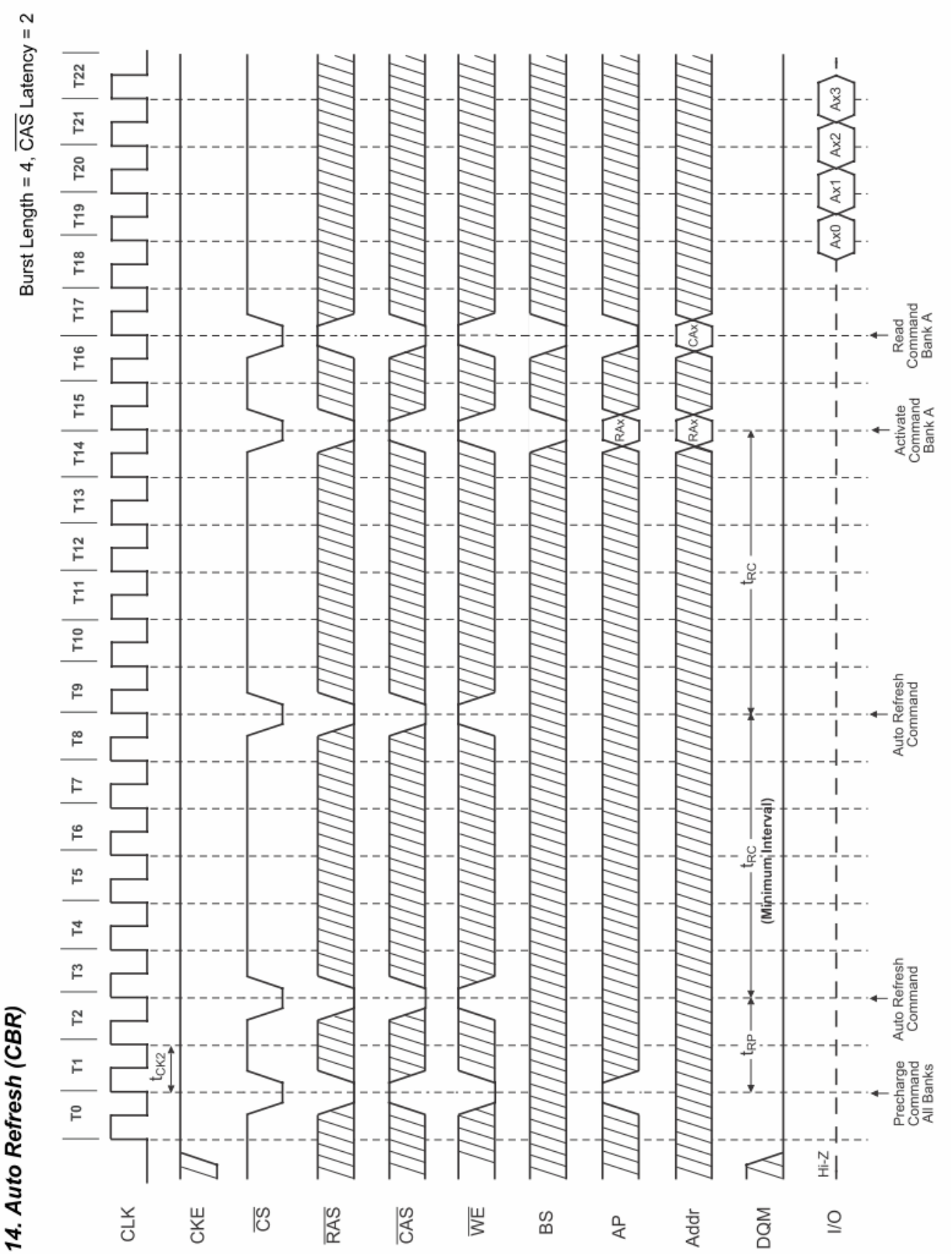
12. Power Down Mode



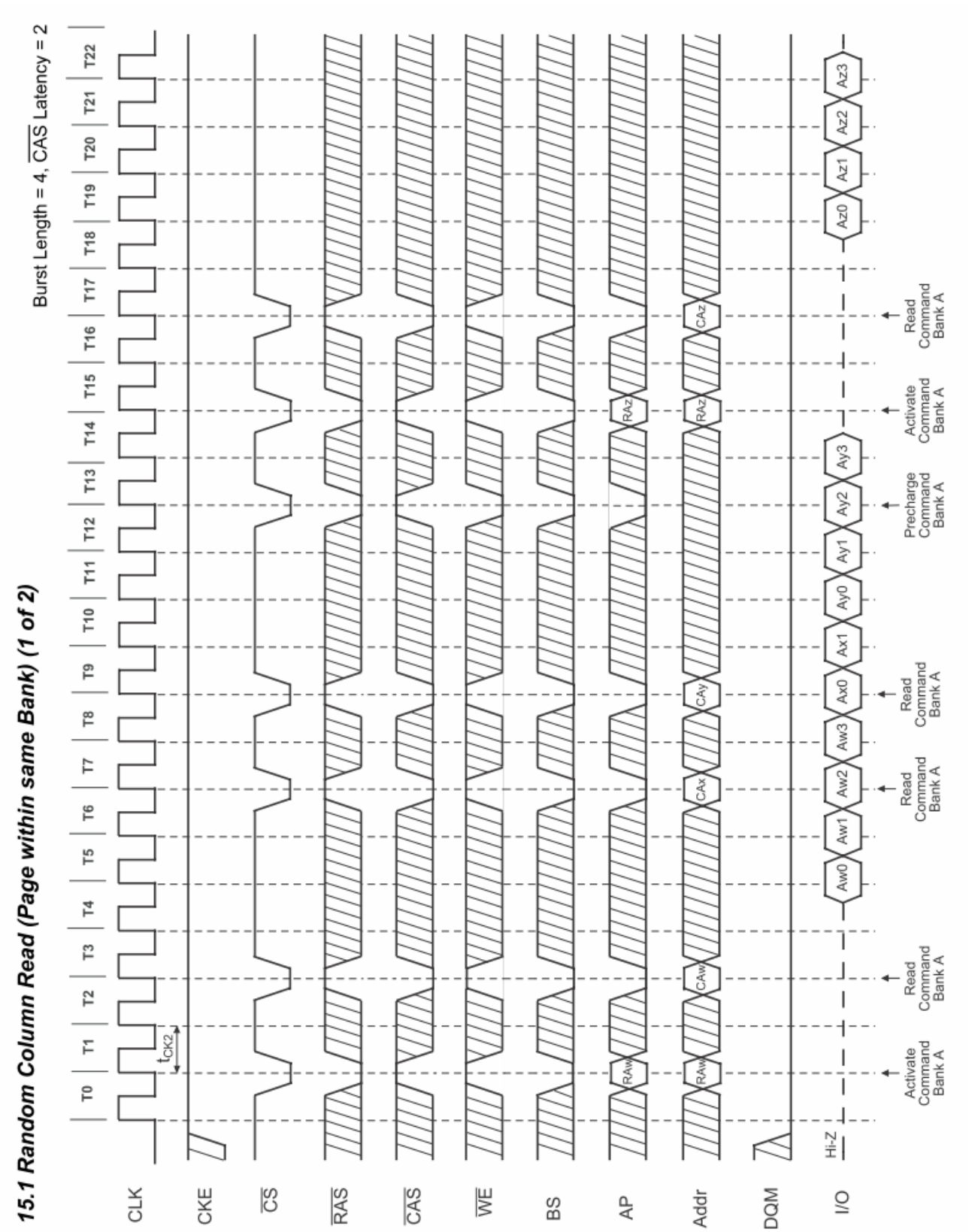
13. Self Refresh (Entry and Exit)



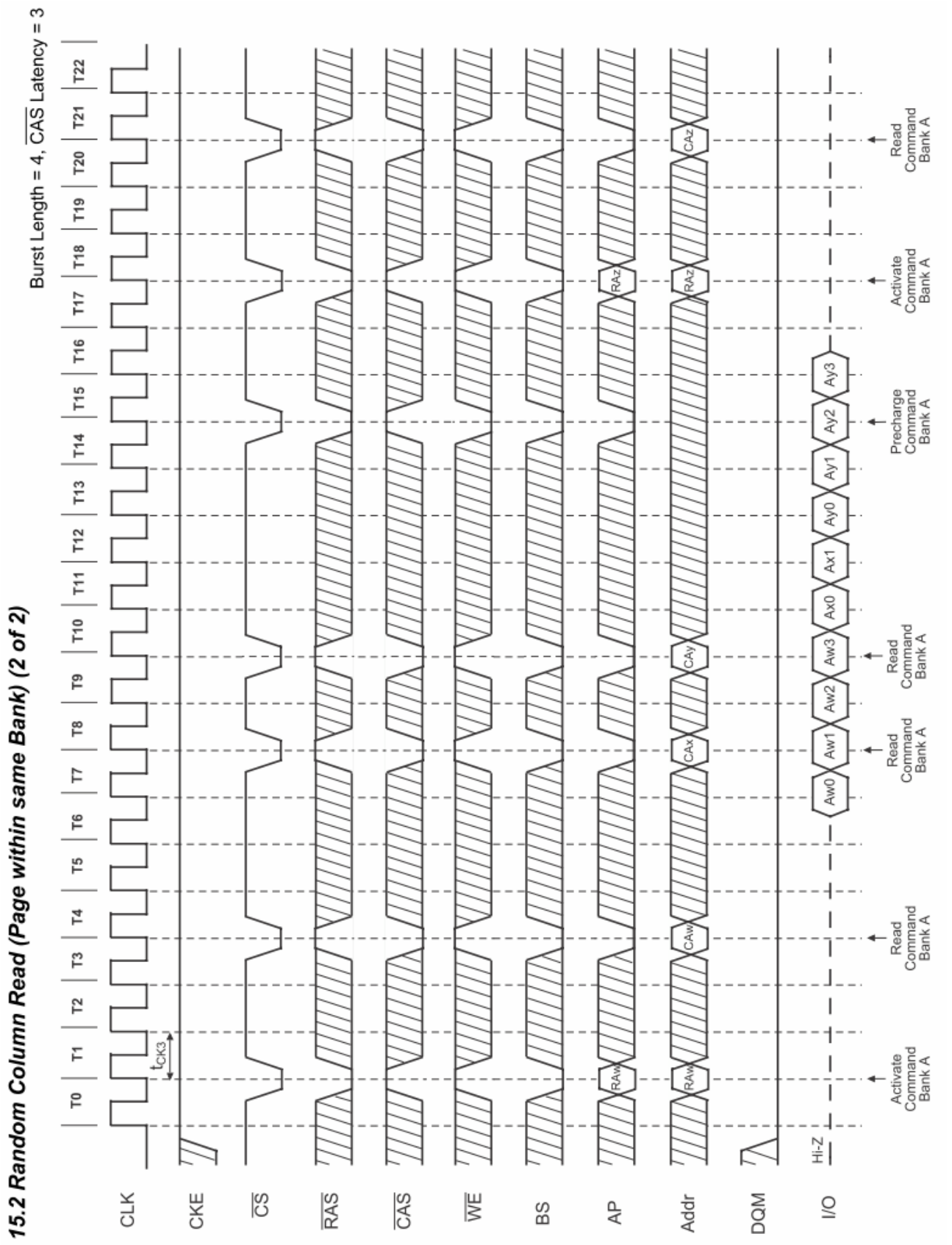
14. Auto Refresh (CBR)



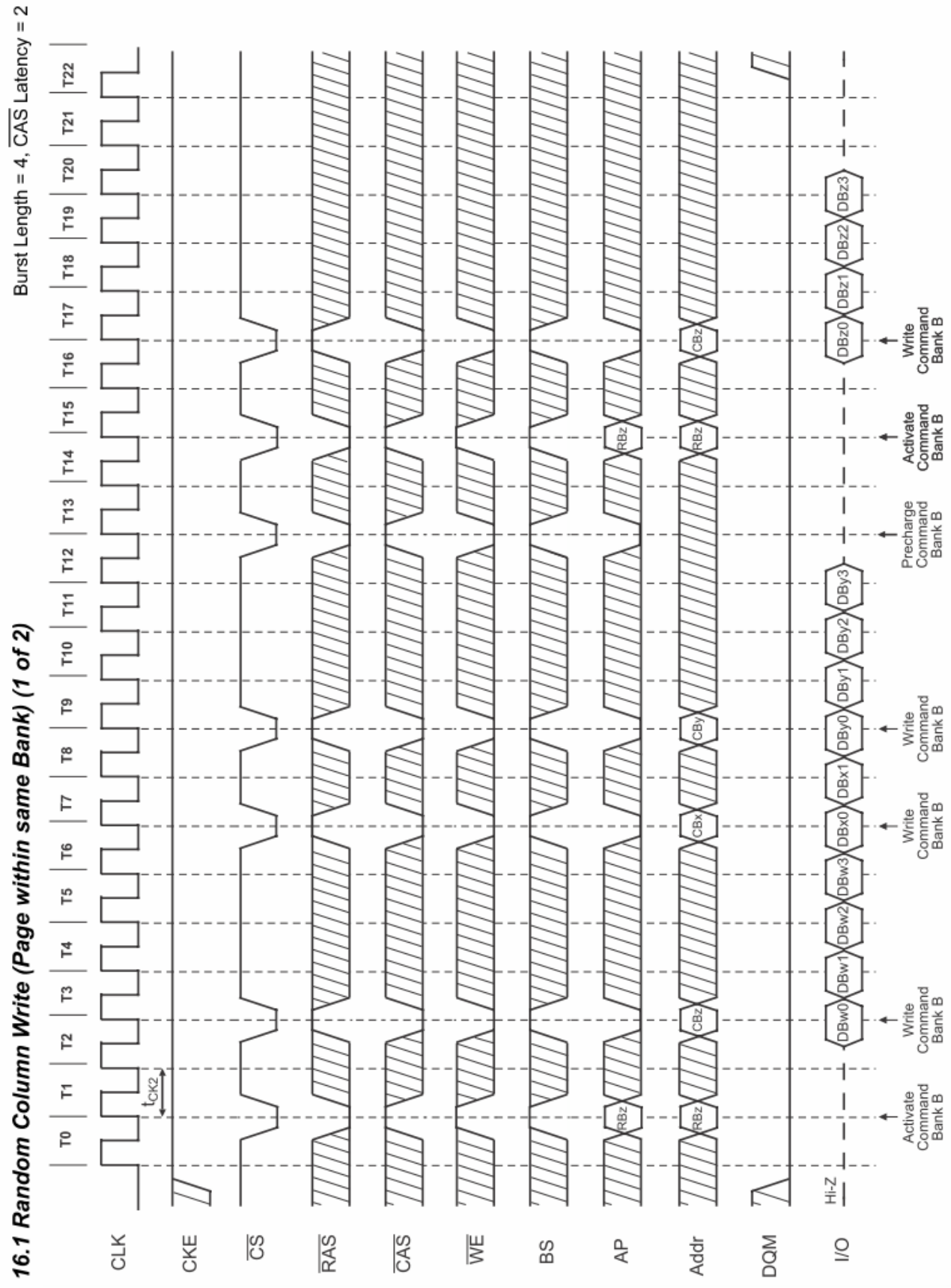
15.1 Random Column Read (Page within same Bank) (1 of 2)



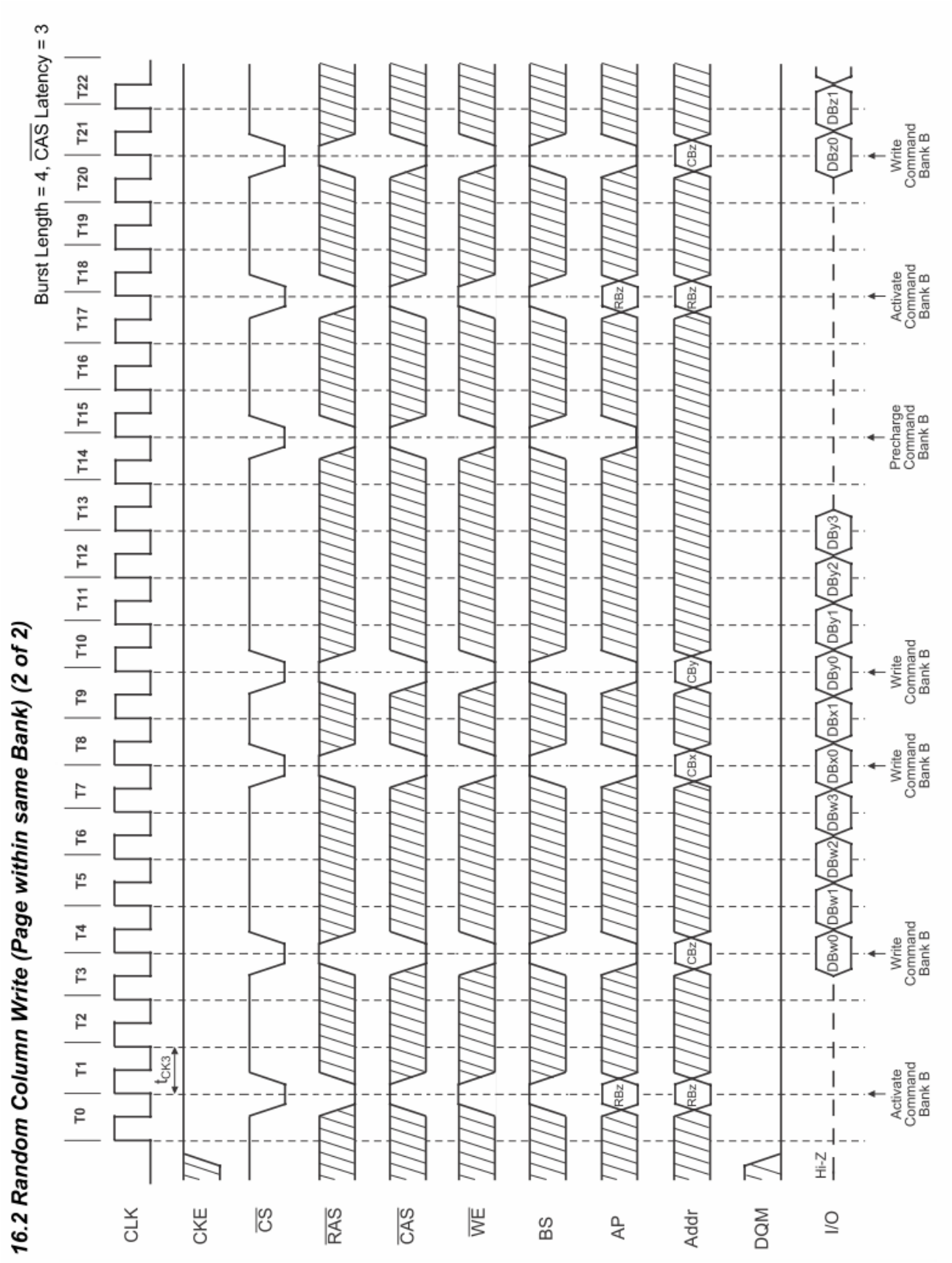
15.2 Random Column Read (Page within same Bank) (2 of 2)



16.1 Random Column Write (Page within same Bank) (1 of 2)

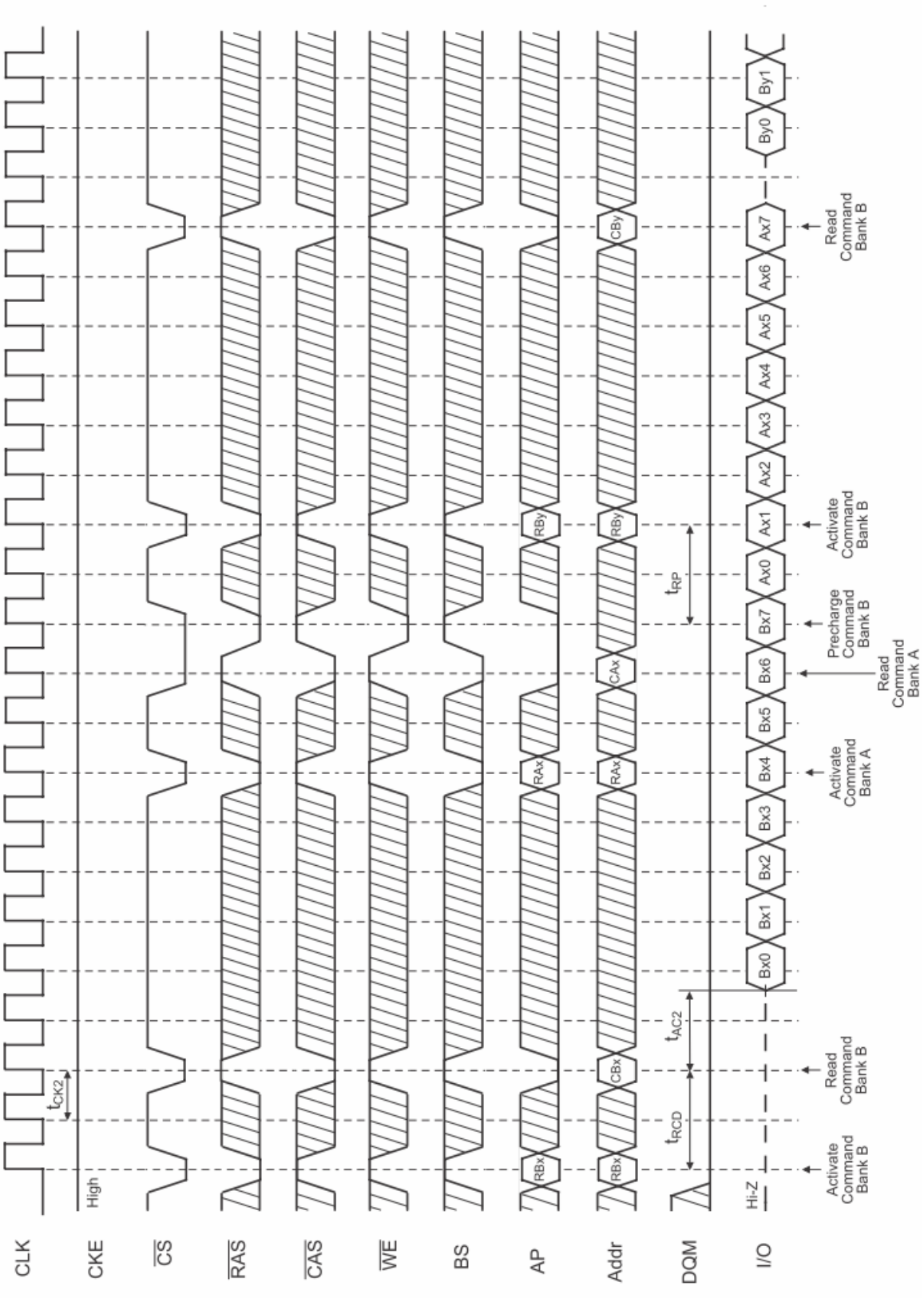


16.2 Random Column Write (Page within same Bank) (2 of 2)



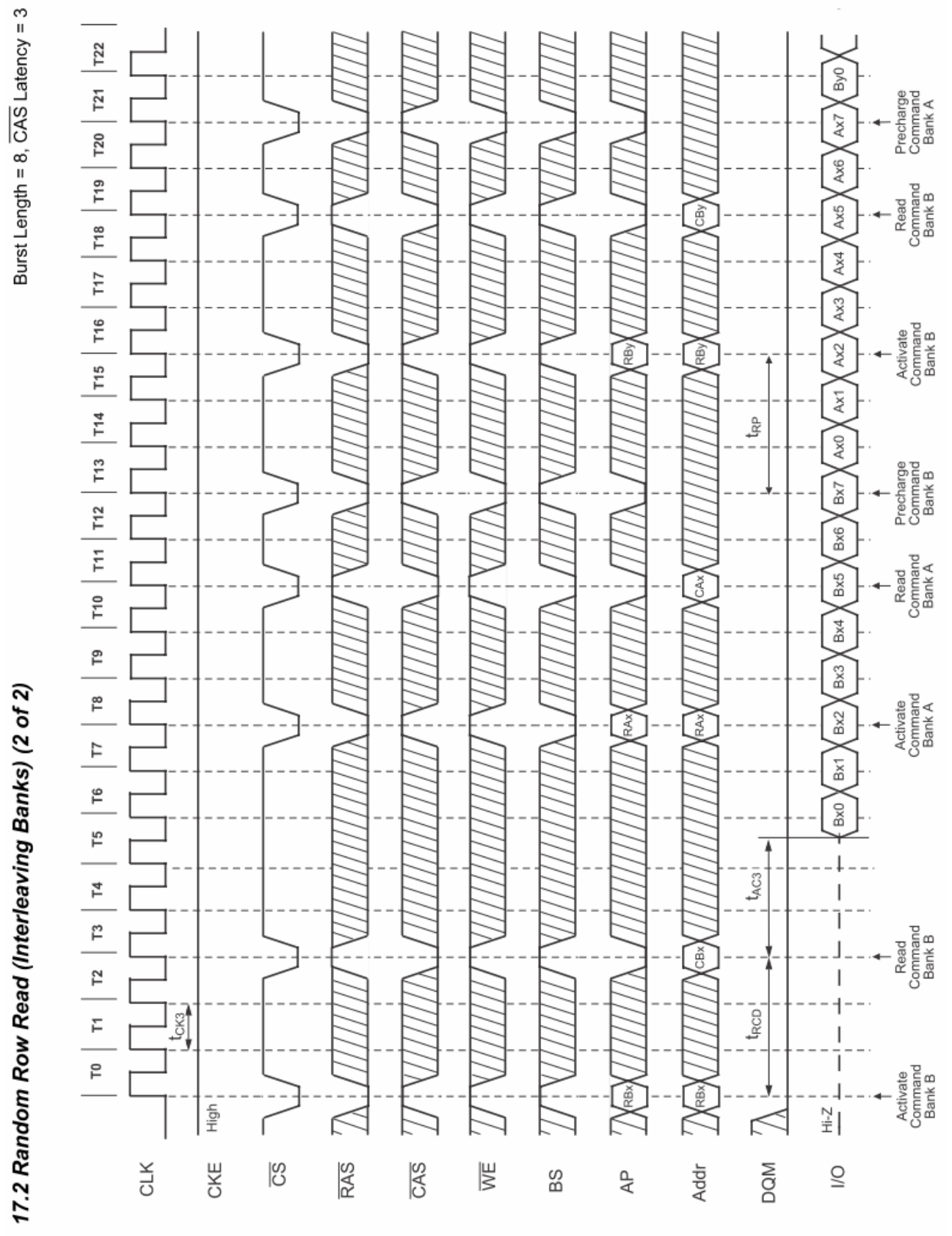
17.1 Random Row Read (Interleaving Banks) (1 of 2)

Burst Length = 8, $\overline{CAS}$ Latency = 2

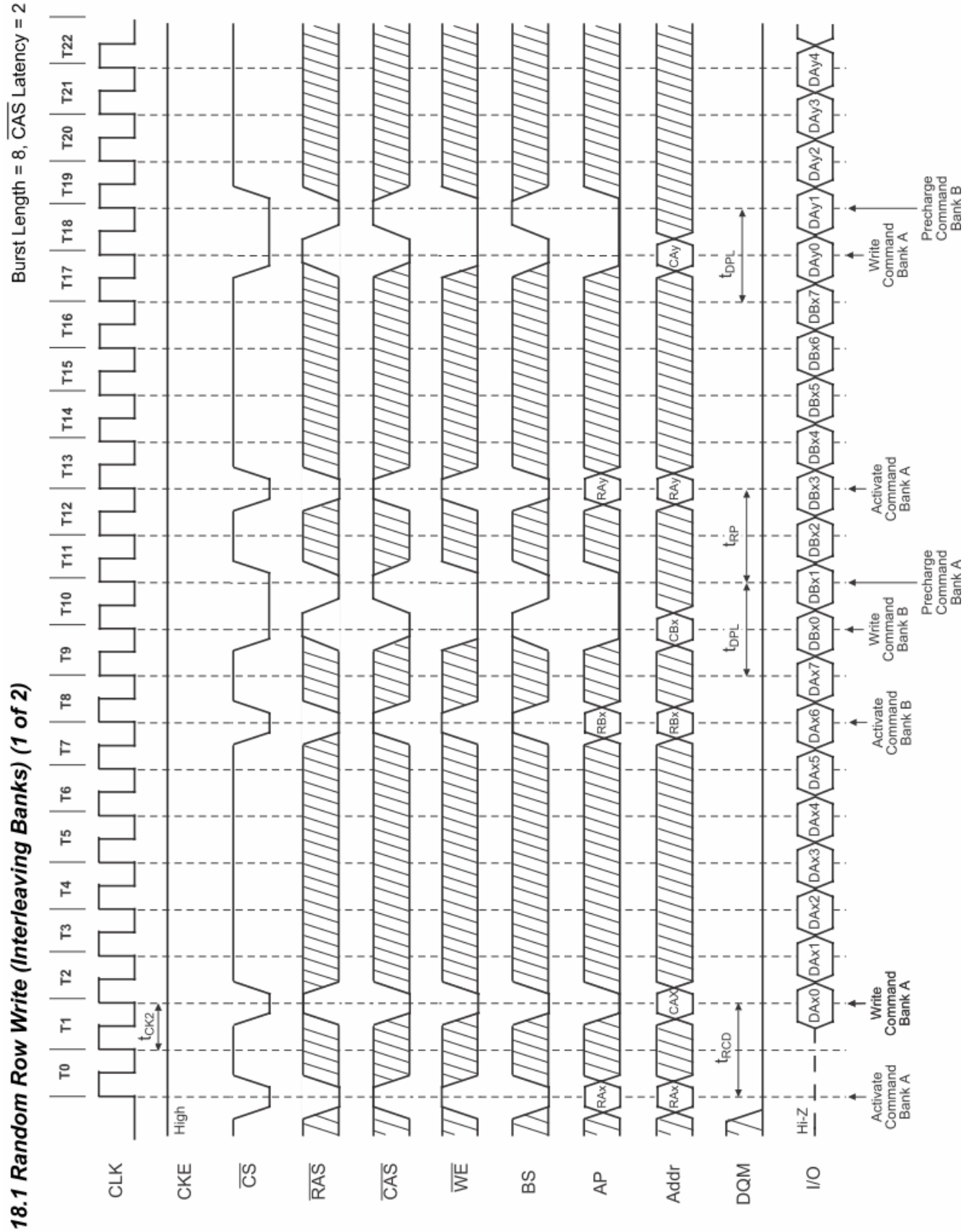


17.2 Random Row Read (Interleaving Banks) (2 of 2)

Burst Length = 8, $\overline{CAS}$ Latency = 3

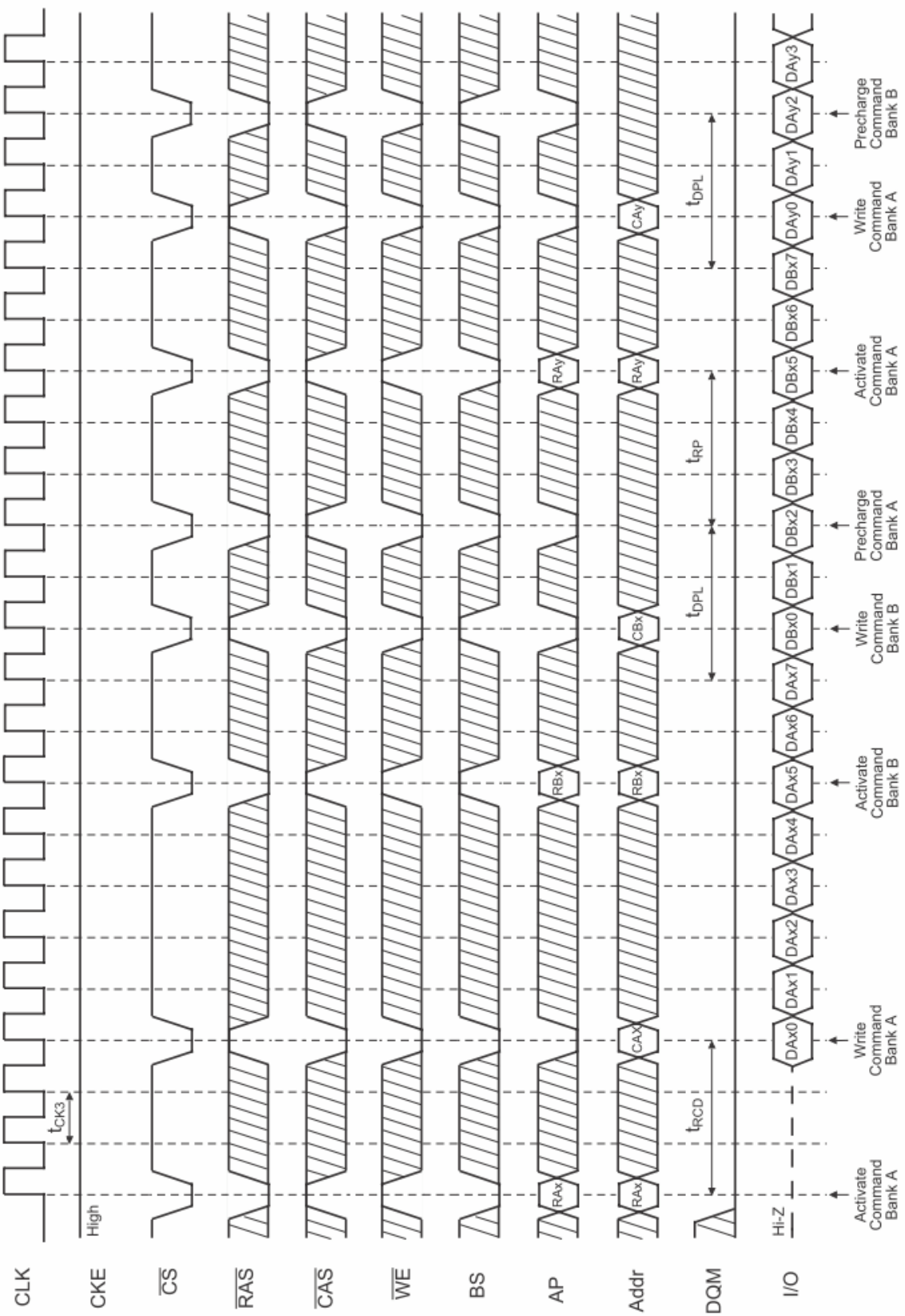


18.1 Random Row Write (Interleaving Banks) (1 of 2)

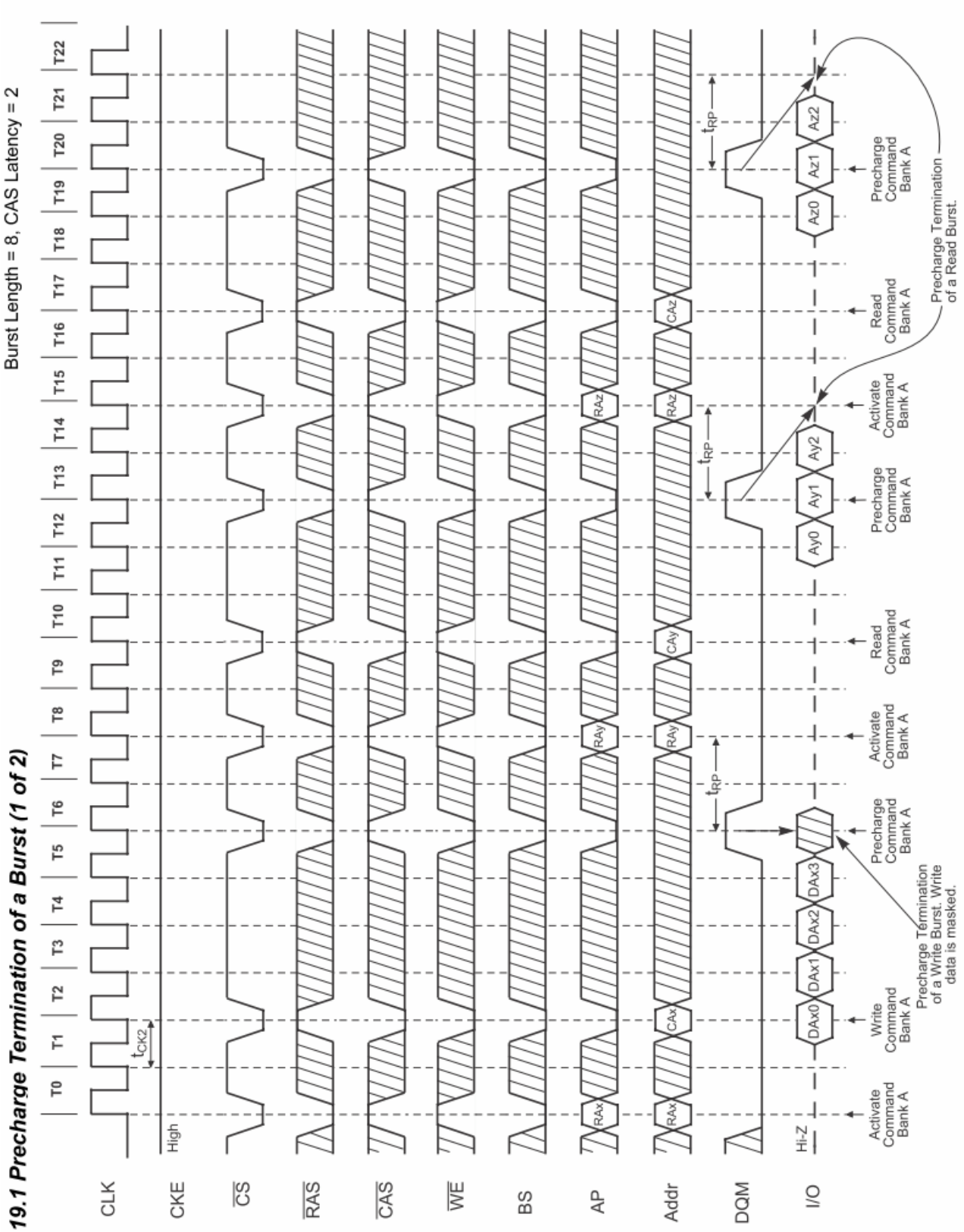


18.2 Random Row Write (Interleaving Banks) (2 of 2)

Burst Length = 8, $\overline{CAS}$ Latency = 3

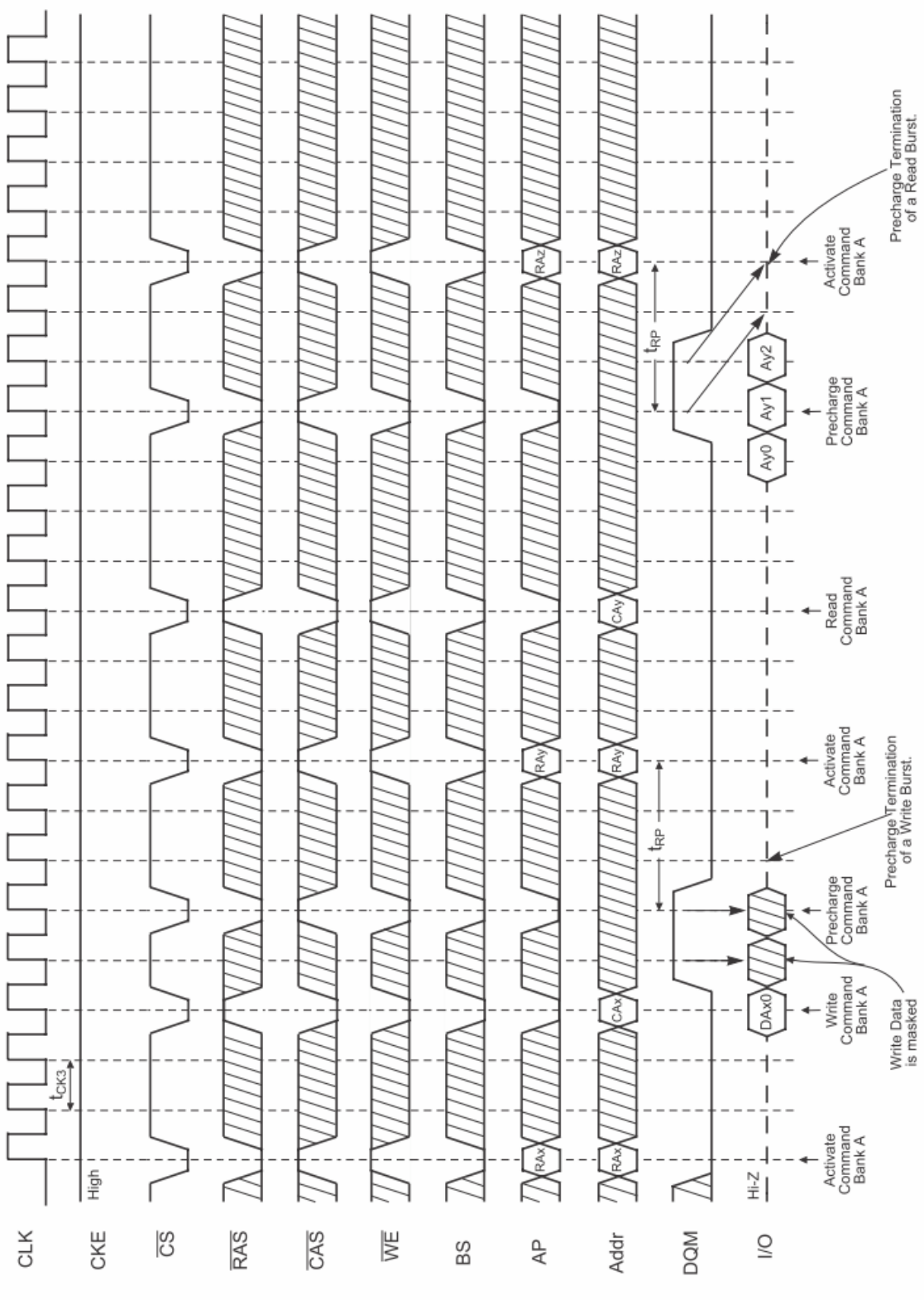


19.1 Precharge Termination of a Burst (1 of 2)



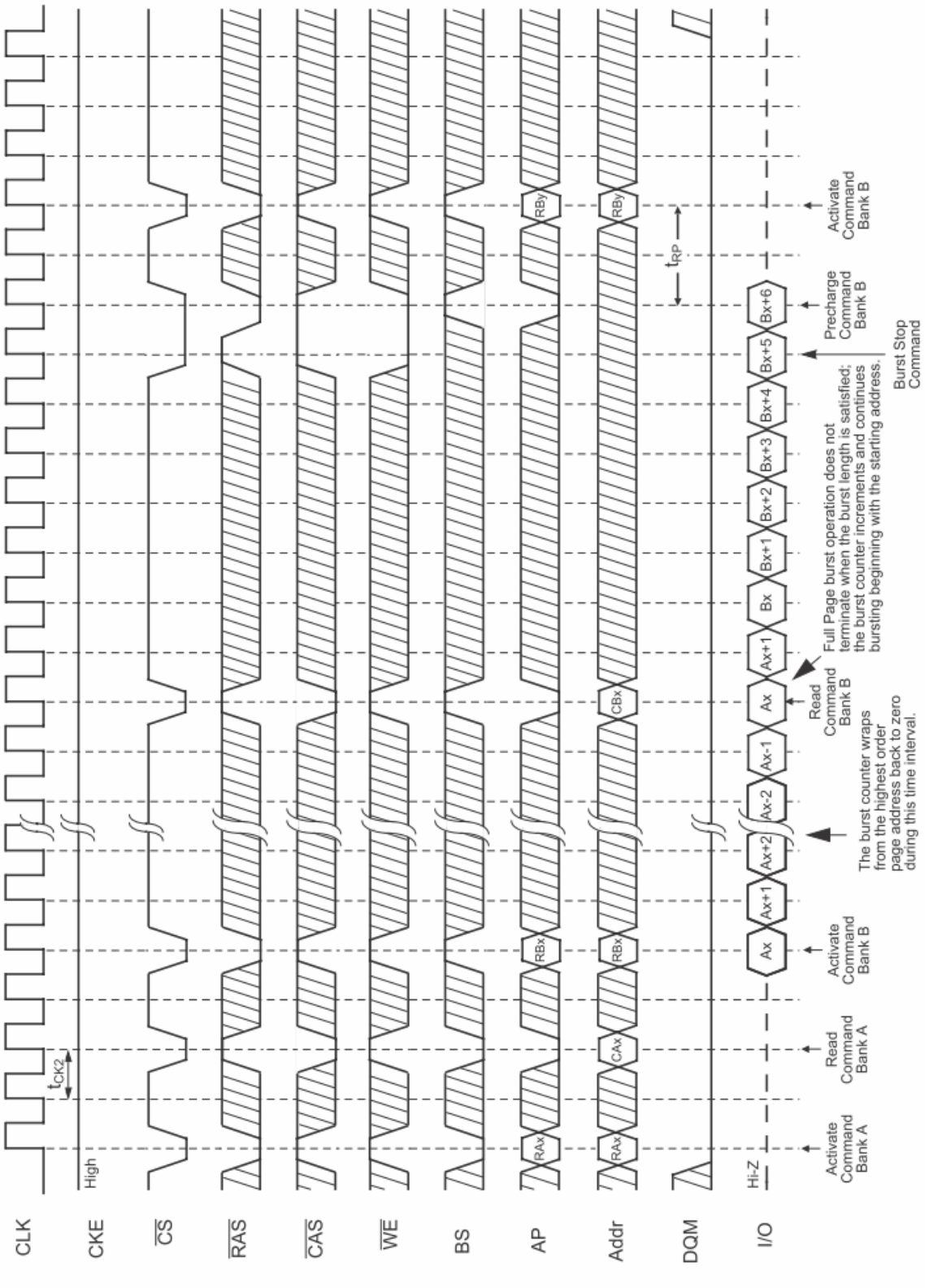
19.2 Precharge Termination of a Burst (2 of 2)

Burst Length = 4, 8, $\overline{CAS}$ Latency = 3

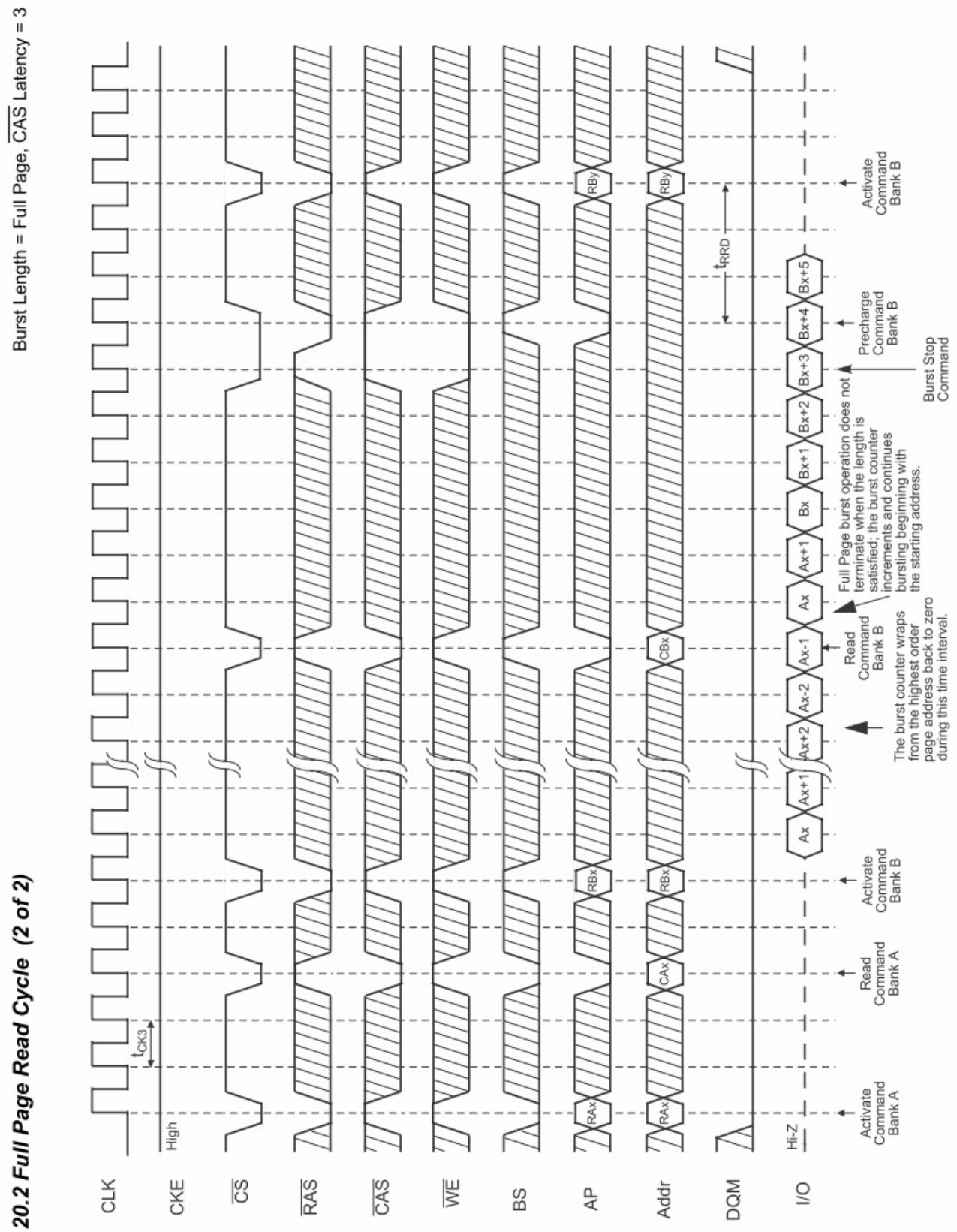


20.1 Full Page Read Cycle (1 of 2)

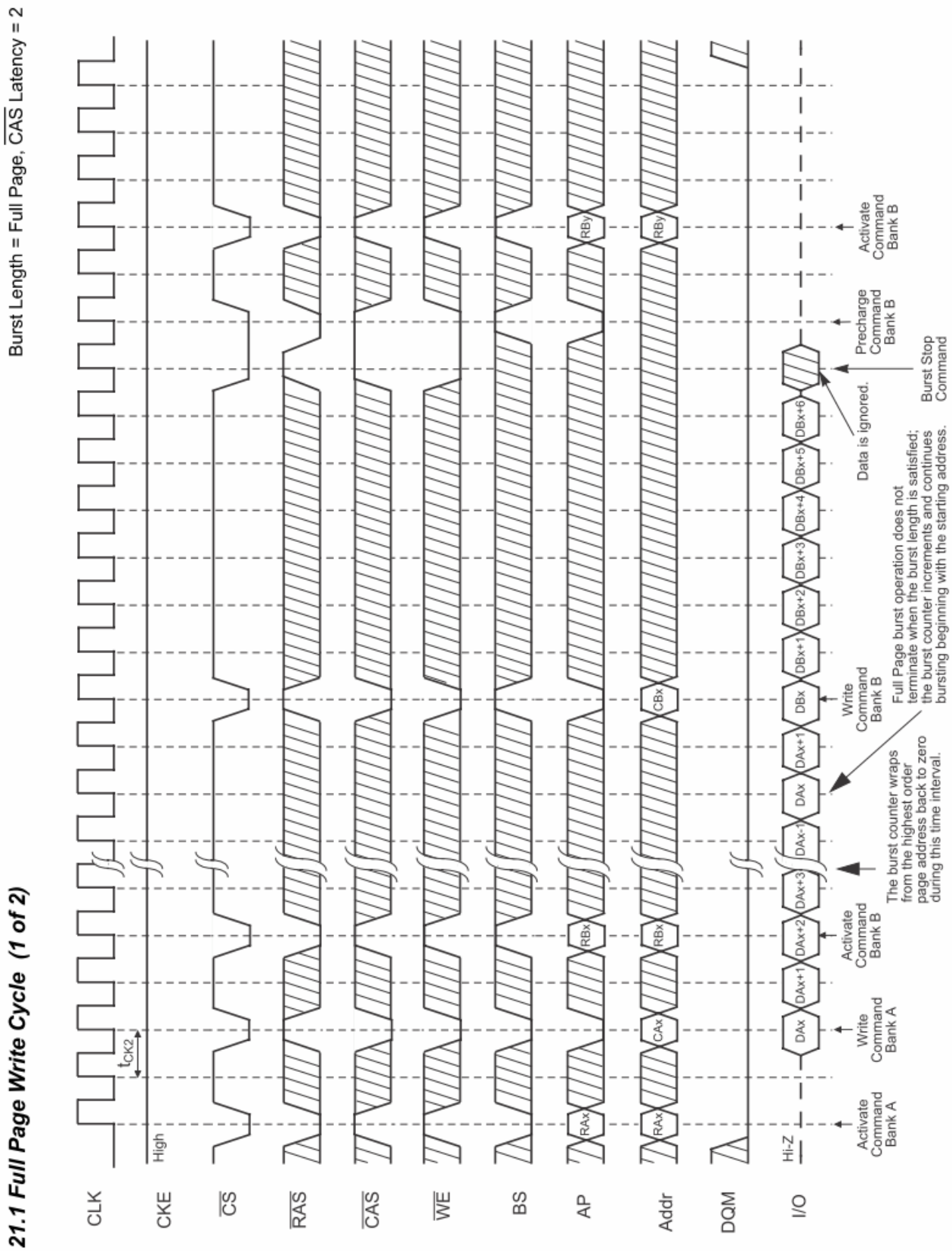
Burst Length = Full Page, $\overline{CAS}$ Latency = 2



20.2 Full Page Read Cycle (2 of 2)

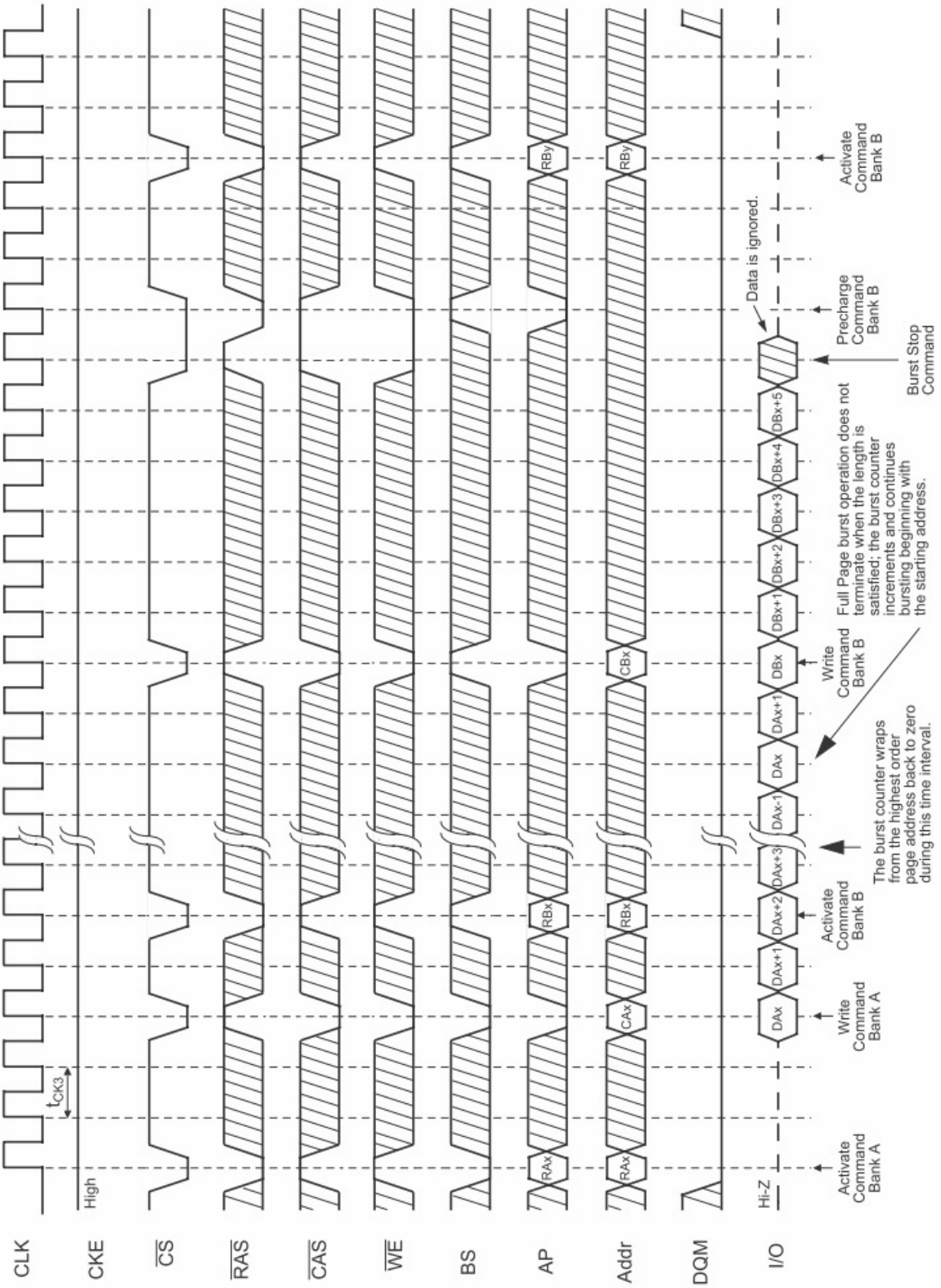


21.1 Full Page Write Cycle (1 of 2)



21.2 Full Page Write Cycle (2 of 2)

Burst Length = Full Page, $\overline{CAS}$ Latency = 3



Complete List of Operation Commands

SDRAM Function Truth Table

CURRENT STATE[1]	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BS	Addr	ACTION
Idle	H	X	X	X	X X	X	NOP or Power Down
	L	H	H	H	BS	X	NOP
	L	H	H	L	BS	X	ILLEGAL[2]
	L	H	L	X	BS	X	ILLEGAL[2]
	L	L	H	H	BS	RA	Row (&Bank) Active; Latch Row Address
	L	L	H	L	X	AP	NOP[4]
	L	L	L	H	Op-	X	Auto-Refresh or Self-Refresh[5]
	L	L	L	L		Code	Mode reg. Access[5]
Row Active	H	X	X	X	X X	X X	NOP
	L	H	H	X	BS	CA,AP	NOP
	L	H	L	H	BS	CA,AP	Begin Read; Latch CA; DetermineAP
	L	H	L	L	BS	X	Begin Write; Latch CA; DetermineAP
	L	L	H	H	BS	AP	ILLEGAL[2]
	L	L	H	L	X	X	Precharge
	L	L	L	X			ILLEGAL
Read	H	X	X	X	X X	X	NOP (Continue Burst to End;>Row Active)
	L	H	H	H	BS	X	NOP (Continue Burst to End;>Row Active)
	L	H	H	L	BS	X	Burst Stop Command > Row Active
	L	H	L	H	BS	CA,AP	Term Burst, New Read, DetermineAP[3]
	L	H	L	L	BS	CA,AP	Term Burst, Start Write, DetermineAP[3]
	L	L	H	H	BS	X	ILLEGAL[2]
	L	L	H	L	X	AP	Term Burst, Precharge
	L	L	L	X		X	ILLEGAL
Write	H	X	X	X	X X	X	NOP (Continue Burst to End;>Row Active)
	L	H	H	H	BS	X	NOP (Continue Burst to End;>Row Active)
	L	H	H	L	BS	X	Burst Stop Command > Row Active
	L	H	L	H	BS	CA,AP	Term Burst, Start Read, DetermineAP[3]
	L	H	L	L	BS	CA,AP	Term Burst, New Write, DetermineAP[3]
	L	L	H	H	BS	X	ILLEGAL[2]
	L	L	H	L	X	AP	Term Burst, Precharge[3]
	L	L	L	X		X	ILLEGAL
Read with Auto Precharge	H	X	X	X	X X	X	NOP (Continue Burst to End;> Precharge)
	L	H	H	H	BS	X	NOP (Continue Burst to End;> Precharge)
	L	H	H	L	BS	X	ILLEGAL[2]
	L	H	L	H	X	X	ILLEGAL[2]
	L	H	L	L	BS	X	ILLEGAL
	L	L	H	H	BS	X	ILLEGAL[2]
	L	L	H	L	X	AP	ILLEGAL[2]
	L	L	L	X		X	ILLEGAL

SDRAM Function Truth Table (continued)

CURRENT STATE[1]	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BS	Addr	ACTION
Write	H	X	X	X	X X	X	NOP (Continue Burst to End;> Precharge)
with	L	H	H	H	BS	X	NOP (Continue Burst to End;> Precharge)
Auto	L	H	H	L	BS	X	ILLEGAL[2]
Precharge	L	H	L	H	X	X	ILLEGAL[2]
	L	H	L	L	BS	X	ILLEGAL
	L	L	H	H	BS	X	ILLEGAL[2]
	L	L	H	L	X	AP	ILLEGAL[2]
	L	L	L	X		X	ILLEGAL
Precharging	H	X	X	X	X X	X	NOP;> Idle after tRP
	L	H	H	H	BS	X	NOP;> Idle after tRP
	L	H	H	L	BS	X	ILLEGAL[2]
	L	H	L	X	BS	X	ILLEGAL[2]
	L	L	H	H	BS	X	ILLEGAL[2]
	L	L	H	L	X	AP	NOP[4]
	L	L	L	X		X	ILLEGAL
Row	H	X	X	X	X X	X	NOP;> Row Active after tRCD
Activating	L	H	H	H	BS	X	NOP;> Row Active after tRCD
	L	H	H	L	BS	X	ILLEGAL[2]
	L	H	L	X	BS	X	ILLEGAL[2]
	L	L	H	H	BS	X	ILLEGAL[2]
	L	L	H	L	X	AP	ILLEGAL[2]
	L	L	L	X		X	ILLEGAL
Write	H	X	X	X	X X	X	NOP NOP
Recovering	L	H	H	H	BS	X	ILLEGAL[2]
	L	H	H	L	BS	X	ILLEGAL[2]
	L	H	L	X	BS	X	ILLEGAL[2]
	L	L	H	H	BS	X	ILLEGAL[2]
	L	L	H	L	X	AP	ILLEGAL
	L	L	L	X		X	
Refreshing	H	X	X	X	X	X	NOP;> Idle after tRC
	L	H	H	H	X	X	NOP;> Idle after tRC
	L	H	H	L	X	X	ILLEGAL
	L	H	L	X	X	X	ILLEGAL
	L	L	H	X	X	X	ILLEGAL
	L	L	L	X	X	X	ILLEGAL
Mode	H	X	X	X	X	X	NOP
Register	L	H	H	H	X	X	NOP
	L	H	H	L	X	X	ILLEGAL
Accessing	L	H	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	ILLEGAL

Clock Enable (CKE) Truth Table:

STATE(n)	CKE n-1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Addr	ACTION
Self-Refresh[6]	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	EXIT Self-Refresh, Idle after tRC
	L	H	L	H	H	H	X	EXIT Self-Refresh, Idle after tRC
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOP (Maintain Self-Refresh)
Power-Down	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	EXIT Power-Down, > Idle.
	L	H	L	H	H	H	X	EXIT Power-Down, > Idle.
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOP (Maintain Low-Power Mode)
All. Banks Idle[7]	H	H	X	X	X	X	X	Refer to the function truth table
	H	L	H	X	X	X	X	Enter Power- Down
	H	L	L	H	H	H	X	Enter Power- Down
	H	L	L	H	H	L	X	ILLEGAL
	H	L	L	H	L	X	X	ILLEGAL
	H	L	L	L	H	X	X	ILLEGAL
	H	L	L	L	L	H	X	Enter Self-Refresh
	H	L	L	L	L	L	X	ILLEGAL
	L	L	X	X	X	X	X	NOP

Abbreviations:

RA = Row Address of Bank A
RB = Row Address of Bank B
RC = Row Address of Bank C
RD = Row Address of Bank D

CA = Column Address of Bank A
CB = Column Address of Bank B
CC = Column Address of Bank C
CD = Column Address of Bank D

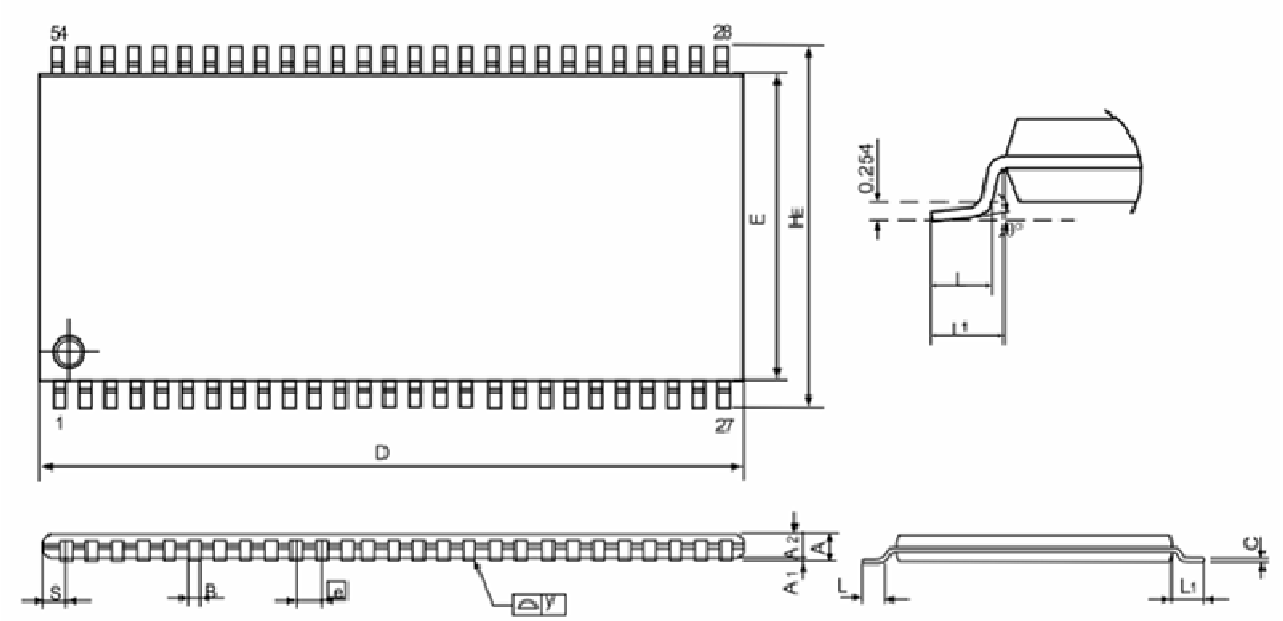
BS = Bank Address
AP = Auto Precharge

Notes for SDRAM function truth table:

1. Current State is state of the bank determined by BS. All entries assume that CKE was active (HIGH) during the preceding clock cycle.
2. Illegal to bank in specified state; Function may be legal in the bank indicated by BS, depending on the state of that bank.
3. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
4. NOP to bank precharging or in Idle state. May precharge bank(s) indicated by BS (andAP).
5. Illegal if any bank is not Idle.
6. CKE Low to High transition will re-enable CLK and other inputs asynchronously. A minimum setup time must be satisfied before any command other than EXIT.
7. Power-Down and Self-Refresh can be entered only from the All Banks Idle State.
8. Must be legal command as defined in the SDRAM function truth table.

Package Diagram

54-Pin Plastic TSOP-II (400 mil)



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	-	-	1.20	-	-	0.047
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
B	0.30	-	0.45	0.012	-	0.018
C	0.12	-	0.21	0.005	-	0.008
D	22.22 BSC			0.875 BSC		
E	10.16 BSC			0.400 BSC		
e	0.80 BSC			0.031 BSC		
HE	11.76 BSC			0.463 BSC		
L	0.40	0.50	0.60	0.016	0.020	0.024
L1	0.80 REF			0.031 REF		
S	0.71 REF			0.028 REF		
y	0.12	-	0.21	0.005	-	0.008
θ	0°	-	8°	0°	-	8°

Revision History

Rev.	History	Release date	Remark
0.1	Initial release	May. 2016	
0.2	Add High Temperature and Extreme Temperature in the Temperature Range	May. 2016	
1.0	Update the value of IDD in IDD specification	Jul. 2016	
2.0	Update timing parameters for -6 speed grade at CL=2	Dec. 2016	
2.1	Revise the remark for Automotive Grade in Option	Nov. 2017	
2.2	Update the table of Capacitance Update the table of Absolute Maximum Ratings Update the table of Signal Pin Description Update the table of Operating Currents Remove the table of Recommended Operation and Characteristics for LV-TTL Add table of DC Characteristics	Aug. 2018	