

# COM Express™ conga-TC570

11th Generation Intel® Core™ i7, i5, i3 and Celeron® Single Chip IOT UP3 Processors

*User's Guide*

Revision 1.00

# Revision History

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Revision	Date (yyyy-mm-dd)	Author	Changes
0.1	2021-05-10	AEM	<ul style="list-style-type: none"><li>• Preliminary release</li></ul>
0.2	2021-07-31	AEM	<ul style="list-style-type: none"><li>• Added Software License Information</li><li>• Removed duplicated sentence about non monotonic voltage in section 5.1.12 "Power Control"</li></ul>
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# Preface

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This user's guide provides information about the components, features, connectors and system resources available on the conga-TC570. It is one of three documents that should be referred to when designing a COM Express™ application. The other reference documents that should be used include the following:

COM Express™ Design Guide

COM Express™ Specification

The links to these documents can be found on the congatec GmbH website at [www.congatec.com](http://www.congatec.com)

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## Terminology

Term	Description
EU	Execution Unit
GB	Gigabyte
GHz	Gigahertz
kB	Kilobyte
MB	Megabyte
Mbit	Megabit
kHz	Kilohertz
MHz	Megahertz
TDP	Thermal Design Power
PCIe	PCI Express
SATA	Serial ATA
PEG	PCI Express Graphics
PCH	Platform Controller Hub
eDP	Embedded DisplayPort
DDI	Digital Display Interface
HDA	High Definition Audio
N.C	Not connected
N.A	Not available
TBD	To be determined
TCC	Time Coordinated Computing
TSN	Time Sensitive Networking

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# 1 Introduction

## 1.1 COM Express™ Concept

COM Express™ is an open industry standard defined specifically for COMs (computer on modules). Its creation makes it possible to smoothly transition from legacy interfaces to the newest technologies available today. COM Express™ modules are available in following form factors:

- Mini 84 mm x 55 mm
- Compact 95 mm x 95 mm
- Basic 125 mm x 95 mm
- Extended 155 mm x 110 mm

Table 1 COM Express™ 3.0 Pinout Types

Types	Connector Rows	PCIe Lanes	PEG	SATA Ports	LAN ports	USB 2.0/ SuperSpeed USB	Display Interfaces
Type 6	A-B C-D	Up to 24	1	Up to 4	1	Up to 8 / 4 <sup>1</sup>	VGA, LVDS/eDP, PEG, 3x DDI
Type 7	A-B C-D	Up to 32	-	Up to 2	5 (1x 1 Gb, 4x 10 Gb)	Up to 4 / 4	
Type 10	A-B	Up to 4	-	Up to 2	1	Up to 8 / 2 <sup>1</sup>	LVDS/eDP, 1x DDI

<sup>1</sup> The SuperSpeed USB ports (USB 3.0) are not in addition to the USB 2.0 ports. Up to 4 of the USB 2.0 ports can support SuperSpeed USB.

The conga-TC570 modules use the Type 6 pinout definition and comply with COM Express 3.0 specification. They are equipped with two high performance connectors that ensure stable data throughput.

The COM integrates all the core components and is mounted onto an application specific carrier board. COM modules are legacy-free design (no Super I/O, PS/2 keyboard and mouse) and provide most of the functional requirements for any application. These functions include, but are not limited to a rich complement of contemporary high bandwidth serial interfaces such as PCI Express, Serial ATA, USB 2.0, and Gigabit Ethernet. The robust thermal and mechanical concept, combined with extended power-management capabilities, is perfectly suited for all applications.

Carrier board designers can use as little or as many of the I/O interfaces as deemed necessary. The carrier board can therefore provide all the interface connectors required to attach the system to the application specific peripherals. This versatility allows the designer to create a dense and optimized package, which results in a more reliable product while simplifying system integration. Most importantly, COM Express™ modules are scalable, which means once an application has been created there is the ability to diversify the product range through the use of different performance class or form factor size modules. Simply unplug one module and replace it with another; no redesign is necessary.

## 1.2 Options Information

The conga-TC570 is currently available in seven variants. The table below shows the different configurations available.

Table 2 conga-TC570 Commercial Variants

Part-No.	050300	050301	050302	050303
Processor	Intel® Core™ i7-1185G7E 1.8 GHz Quad Core™	Intel® Core™ i5-1145G7E 1.5 GHz Quad Core™	Intel® Core™ i3-1115G4E 2.2 GHz Dual Core™	Intel® Celeron® 6305E 1.8 GHz Dual Core
Intel® Smart Cache	12 MB	8 MB	6 MB	4 MB
Max. Turbo Frequency	4.4 GHz	4.1 GHz	3.9 GHz	N.A
Processor Graphics	Intel® Iris® Xe (with 96 EU)	Intel® Iris® Xe (with 80 EU)	Intel® UHD Graphics (with 48 EU)	Intel® UHD Graphics (with 48 EU)
GFX Base/Max. Dynamic Freq.	1.35 GHz	1.30 GHz	1.25 GHz	1.25 GHz
DDR4 Memory (ECC or Non-ECC)	3200 MTps dual channel Non-ECC	3200 MTps dual channel Non-ECC	3200 MTps dual channel Non-ECC	3200 MTps dual channel Non-ECC
Processor TDP (cTDP down)	15 (12) W	15 (12) W	15 (12) W	15 W (N.A)

Table 3 conga-TC570 Industrial Variants

Part-No.	050310	050311	050312
Processor	Intel® Core™ i7-1185GRE 1.8 GHz Quad Core™	Intel® Core™ i5-1145GRE 1.5 GHz Quad Core™	Intel® Core™ i3-1115GRE 2.2 GHz Dual Core™
Intel® Smart Cache	12 MB	8 MB	6 MB
Max. Turbo Frequency	4.4 GHz	4.1 GHz	3.9 GHz
Processor Graphics	Intel® Iris® Xe (with 96 EU)	Intel® Iris® Xe (with 80 EU)	Intel® UHD Graphics (with 48 EU)
GFX Base/Max. Dynamic Freq.	1.35 GHz	1.35 GHz	1.25 GHz
DDR4 Memory (ECC or Non-ECC)	3200 MTps dual channel InBand ECC (IBECC)	3200 MTps dual channel InBand ECC (IBECC)	3200 MTps dual channel InBand ECC (IBECC)
Processor TDP (cTDP down)	15 (12) W	15 (12) W	15 (12) W

## 2 Specifications

### 2.1 Feature List

Table 4 Feature Summary

<b>Form Factor</b>	Based on COM Express™ standard pinout Type 6 Rev. 3.0 (Compact size 95 x 95 mm)	
<b>Processor</b>	11 <sup>th</sup> Generation Intel® Core™ i7,i5, i3 and Celeron® Single Chip IOT UP3 Processors	
<b>Memory</b>	Two memory sockets (located on the top and bottom side of the conga-TC570) with support for: <ul style="list-style-type: none"> <li>- SO-DIMM non-ECC DDR4 modules</li> <li>- Data rates up to 3200 MTps</li> <li>- Maximum 64 GB capacity (32 GB each)</li> <li>- InBand ECC <sup>1</sup> (out-of-band ECC is not supported)</li> </ul>	
<b>Chipset</b>	Intel® 500 Series PCH-LP integrated in the Multi-Chip Package	
<b>Audio</b>	High Definition Audio interface with support for multiple codecs	
<b>Ethernet</b>	Intel® i225 LM/V/IT 2.5 GbE controller with support for TSN	
<b>Graphics Options</b>	Intel® Iris® Xe (Gen. 12). Supports: <ul style="list-style-type: none"> <li>- API (DirectX 12, Direct3D 12, Direct3D 2015, OpenGL 4.5, OpenCL 2.2)</li> <li>- Intel® QuickSync &amp; Clear Video Technology HD (hardware accelerated video decode/encode/processing/transcode)</li> <li>- Up to four independent displays (see table 10 "Display Combination and Resolution")</li> </ul>	
	3x DP++ 1x LVDS/eDP <sup>2</sup> 1x PEG x4 port (PCIe Gen 4)	1x VGA <sup>3</sup> Resolutions up to 4x4K @ 60 Hz
<b>Peripheral Interfaces</b>	8x USB 2.0 (Up to 4x USB 3.2 Gen 2x1) Up to 2x SATA® 6 with RAID 0/1/5 (shared with PCIe5 and PCIe6) <sup>4</sup> Up to 8x PCI Express® Gen. 3 lanes <sup>4</sup> 2x UART (16C550 compatible) GPIOs	LPC I <sup>2</sup> C (fast mode, multi-master) SMB SPI
<b>BIOS</b>	AMI Aptio® V UEFI 2.x firmware 32 MB serial SPI flash with congatec Embedded BIOS features	
<b>Power Management</b>	ACPI 4.0a compliant with battery support. S5e mode (see section 6.1.7 "Enhanced Soft-Off State") Deep Sx and Suspend to RAM (S3) Configurable TDP	
<b>congatec Board Controller</b>	Multi-stage watchdog, non-volatile user data storage, manufacturing and board information, board statistics, hardware monitoring, fan control, I2C bus, Power loss control	
<b>Security</b>	Discrete SPI Trusted Platform Module (Infineon SLB9670VQ2.0); AES Instructions	



## 2.4 Supply Voltage Standard Power

- 8 V – 20 V DC

### 2.4.1 Electrical Characteristics

Power supply pins on the module's connectors limit the amount of input power. The following table provides an overview of the limitations for pinout Type 6 (dual connector, 440 pins).

Table 5 Overview of Type 6 Limitations

Power Rail	Module Pin Current Capability (Ampere)	Nominal Input (Volts)	Input Range (Volts)	Derated Input (Volts)	Max. Input Ripple (10Hz to 20MHz) (mV)	Max. Module Input Power (w. derated input) (Watts)	Assumed Conversion Efficiency	Max. Load Power (Watts)
VCC_12V	12	12	11.4-12.6	11.4	+/- 100	137	85%	116
VCC_5V-SBY	2	5	4.75-5.25	4.75	+/- 50	9		
VCC_RTC	0.5	3	2.5-3.3		+/- 20			

### 2.4.2 Rise Time

The input voltages shall rise from 10 percent of nominal to 90 percent of nominal at a minimum slope of 250 V/s. The smooth turn-on requires that, during the 10 percent to 90 percent portion of the rise time, the slope of the turn-on waveform must be positive.

## 2.5 Power Consumption

The power consumption values were measured with the following setup:

- Input voltage +12 V
- conga-TC570 COM
- Modified congatec carrier board
- conga-TC570 cooling solution
- Microsoft Windows 10 (64 bit)



### Note

*The CPU was stressed to its maximum workload with the Intel® Thermal Analysis Tool*

**Table 6 Measurement Description**

The power consumption values were recorded during the following system states:

System State	Description	Comment
S0: Minimum value	Lowest frequency mode (LFM) with minimum core voltage during desktop idle	
S0: Maximum value	Highest frequency mode (HFM/Turbo Boost)	The CPU was stressed to its maximum frequency
S0: Peak current	Highest current spike during the measurement of "S0: Maximum value". This state shows the peak value during runtime.	Consider this value when designing the system's power supply to ensure that sufficient power is supplied during worst case scenarios
S3	COM is powered by VCC_5V_SBY	
S5	COM is powered by VCC_5V_SBY	
S5e	COM is powered by VCC_5V_SBY	



### Note

1. *The fan and SATA drives were powered externally.*
2. *All other peripherals except the LCD monitor were disconnected before measurement*

**Table 7 Power Consumption Values (Nominal TDP and TDP Up)**

The tables below provide additional information about the conga-TC570 power consumption. The values were recorded at various operating modes.

**Nominal TDP (15 W TDP)**

Part No.	Memory Size	H.W Rev.	BIOS Rev.	OS (64 bit)	CPU			Current (Ampere)					
					Variant	Cores	Freq. /Turbo (GHz)	S0: Min	S0: Max	S0: Peak	S3	S5	S5e
050300	2 x 4 GB	A.2	BVTLR009	Windows 10	Intel® Core™ i7-1185G7E	4	1.8 / 4.4	0.52	1.95	6.78	0.11	0.08	0.000105
050301	2 x 4 GB	A.2	BVTLR009	Windows 10	Intel® Core™ i5-1145G7E	4	1.5 / 4.1	0.52	2.12	6.55	0.11	0.09	0.000105
050302	2 x 4 GB	A.2	BVTLR009	Windows 10	Intel® Core™ i3-1115G4E	2	2.2 / 3.9	0.53	1.97	3.32	0.16	0.09	0.000105
050303	2 x 4 GB	A.2	BVTLR009	Windows 10	Intel® Celeron® 6305E	2	1.8 / N.A	0.43	1.25	1.41	0.11	0.09	0.000105
050310	2 x 4 GB	A.2	BVTLR009	Windows 10	Intel® Core™ i7-1185GRE	4	1.8 / 4.4	0.51	2.13	6.91	0.11	0.08	0.000105
050311	2 x 4 GB	A.2	BVTLR009	Windows 10	Intel® Core™ i5-1145GRE	4	1.5 / 4.1	0.44	2.03	6.62	0.10	0.08	0.000105
050312	2 x 4 GB	A.2	BVTLR009	Windows 10	Intel® Core™ i3-1115GRE	2	2.2 / 3.9	0.50	2.04	3.44	0.11	0.08	0.000105

**TDP Up (28 W TDP)**

Part No.	Memory Size	H.W Rev.	BIOS Rev.	OS (64 bit)	CPU			Current (Ampere)					
					Variant	Cores	Freq. /Turbo (GHz)	S0: Min	S0: Max	S0: Peak	S3	S5	S5e
050300	2 x 4 GB	A.2	BVTLR009	Windows 10	Intel® Core™ i7-1185G7E	4	1.8 / 4.4	0.51	4.09	7.14	0.11	0.08	0.000105
050301	2 x 4 GB	A.2	BVTLR009	Windows 10	Intel® Core™ i5-1145G7E	4	1.5 / 4.1	0.51	4.07	6.94	0.11	0.09	0.000105
050302	2 x 4 GB	A.2	BVTLR009	Windows 10	Intel® Core™ i3-1115G4E	2	2.2 / 3.9	0.53	3.22	3.47	0.16	0.09	0.000105
050310	2 x 4 GB	A.2	BVTLR009	Windows 10	Intel® Core™ i7-1185GRE	4	1.8 / 4.4	0.48	4.20	6.74	0.11	0.09	0.000105
050311	2 x 4 GB	A.2	BVTLR009	Windows 10	Intel® Core™ i5-1145GRE	4	1.5 / 4.1	0.46	4.18	6.85	0.11	0.08	0.000105
050312	2 x 4 GB	A.2	BVTLR009	Windows 10	Intel® Core™ i3-1115GRE	2	2.2 / 3.9	0.45	3.30	3.52	0.10	0.08	0.000105

## 2.6 Supply Voltage Battery Power

Table 8 CMOS Battery Power Consumption

RTC @	Voltage	Current
-10°C	3V DC	1.37 $\mu$ A
20°C	3V DC	2.33 $\mu$ A
70°C	3V DC	2.79 $\mu$ A

### Note

1. Do not use the CMOS battery power consumption values listed above to calculate CMOS battery lifetime.
2. Measure the CMOS battery power consumption of your application in worst case conditions (for example, during high temperature and high battery voltage).
3. Consider the self-discharge of the battery when calculating the lifetime of the CMOS battery. For more information, refer to application note AN9\_RTC\_Battery\_Lifetime.pdf on congatec GmbH website at [www.congatec.com/support/application-notes](http://www.congatec.com/support/application-notes).
4. We recommend to always have a CMOS battery present when operating the conga-TC570.

## 2.7 Environmental Specifications

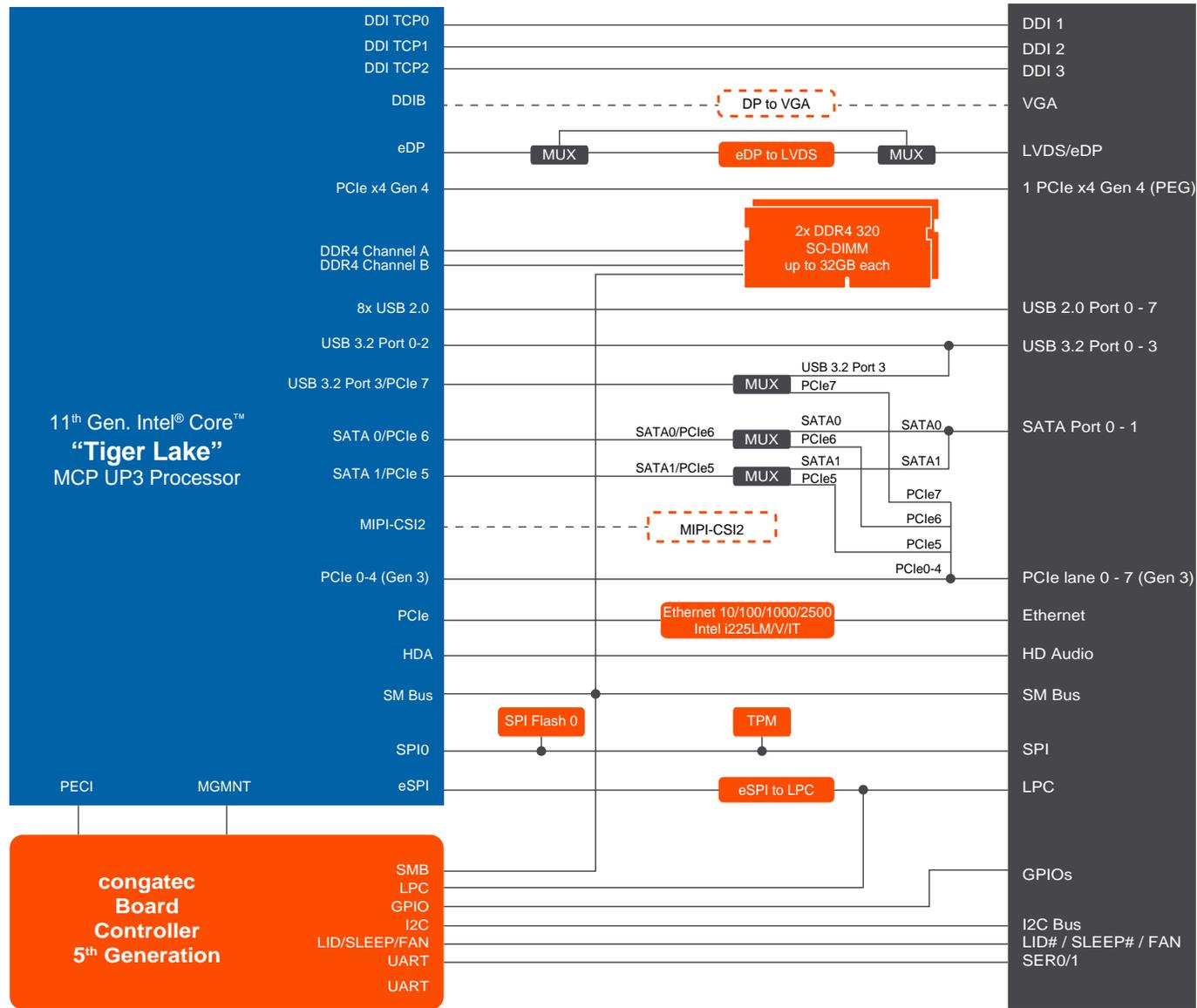
Temperature (commercial variants)	Operation: 0° to 60°C	Storage: -20° to +80°C
Temperature (industrial variants)	Operation: -40° to 85°C	Storage: -40° to +85°C
Humidity	Operation: 10% to 90%	Storage: 5% to 95%

### Caution

The above operating temperatures must be strictly adhered to at all times. When using a congatec heatspreader, the maximum operating temperature refers to any measurable spot on the heatspreader's surface.

Humidity specifications are for non-condensing conditions.

# 3 Block Diagram



 Optional - Not available by default

## 4 Cooling Solutions

congatec GmbH offers the following cooling solutions for the conga-TC570. The dimensions of the cooling solutions are shown in the sub-sections. All measurements are in millimeters.

Table 9 Cooling Solution Variants

	Cooling Solution	Part No	Description
1	CSA	050350	Active cooling solution with integrated heat pipes and 2.7 mm bore-hole standoffs
		050351	Active cooling with integrated heat pipes and M2.5 mm threaded standoffs
2	CSP	050352	Passive cooling solution with integrated heat pipes and 2.7 mm bore-hole standoffs
		050353	Passive cooling solution with integrated heat pipes and M2.5 mm threaded standoffs
3	HSP	050354	Heatspreader with integrated heat pipes and 2.7 mm bore-hole standoffs
		050355	Heatspreader with with integrated heat pipes and M2.5 mm threaded standoffs

### Note

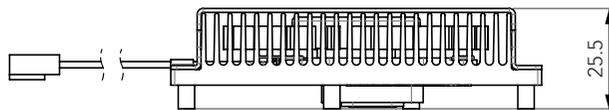
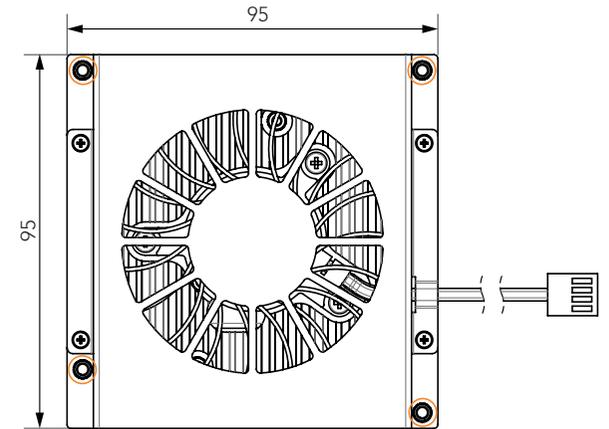
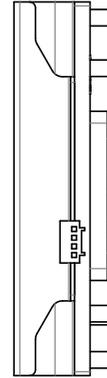
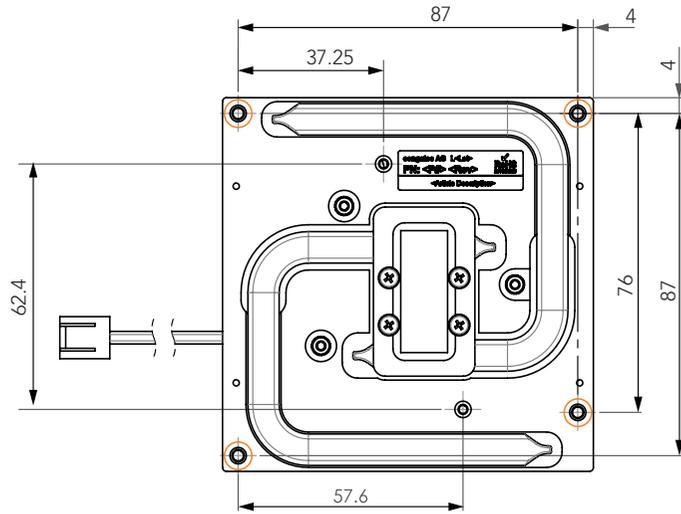
1. We recommend a maximum torque of 0.4 Nm for carrier board mounting screws and 0.5 Nm for module mounting screws.
2. The gap pad material used on congatec heatspreaders may contain silicon oil that can seep out over time depending on the environmental conditions it is subjected to. For more information about this subject, contact your local congatec sales representative and request the gap pad material manufacturer's specification.



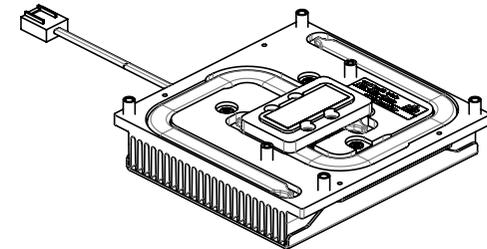
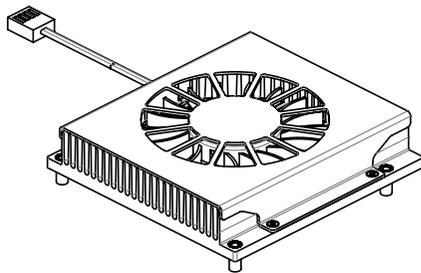
### Caution

1. The congatec heatspreaders/cooling solutions are tested only within the commercial temperature range of 0° to 60°C. Therefore, if your application that features a congatec heatspreader/cooling solution operates outside this temperature range, ensure the correct operating temperature of the module is maintained at all times. This may require additional cooling components for your final application's thermal solution.
2. For adequate heat dissipation, use the mounting holes on the cooling solution to attach it to the module. Apply thread-locking fluid on the screws if the cooling solution is used in a high shock and/or vibration environment. To prevent the standoff from stripping or cross-threading, use non-threaded carrier board standoffs to mount threaded cooling solutions.
3. For applications that require vertically-mounted cooling solution, use only coolers that secure the thermal stacks with fixing post. Without the fixing post feature, the thermal stacks may move.
4. Do not exceed the recommended maximum torque. Doing so may damage the module or the carrier board, or both.

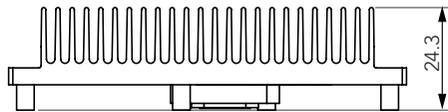
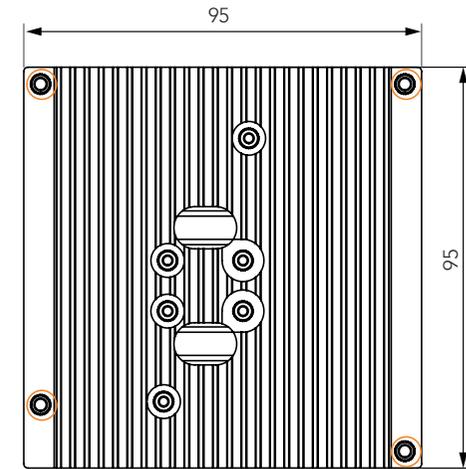
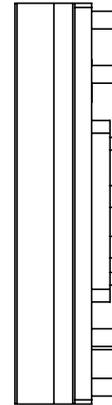
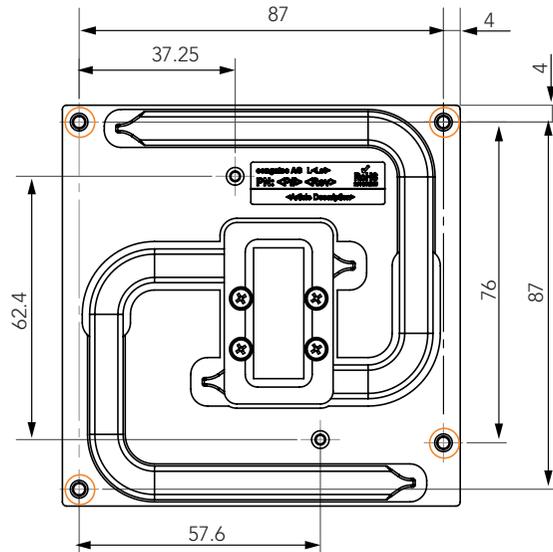
## 4.1 CSA Dimensions



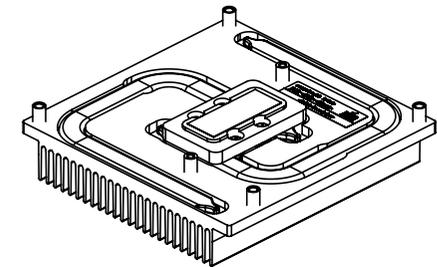
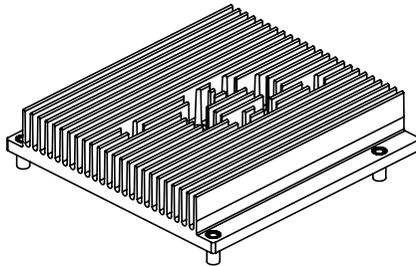
-  M2.5 x 11 mm threaded standoff for threaded version or  $\varnothing 2.7 \times 11$  mm non-threaded standoff for borehole version



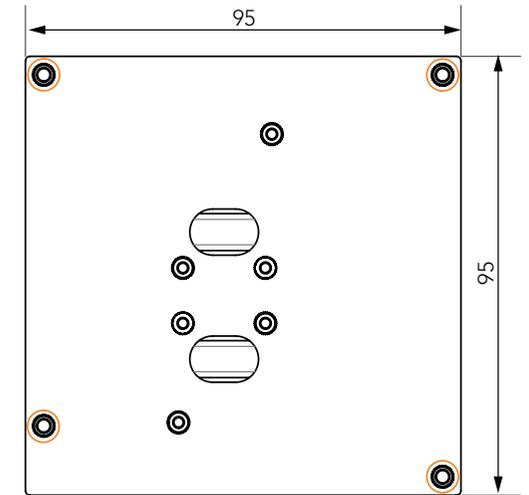
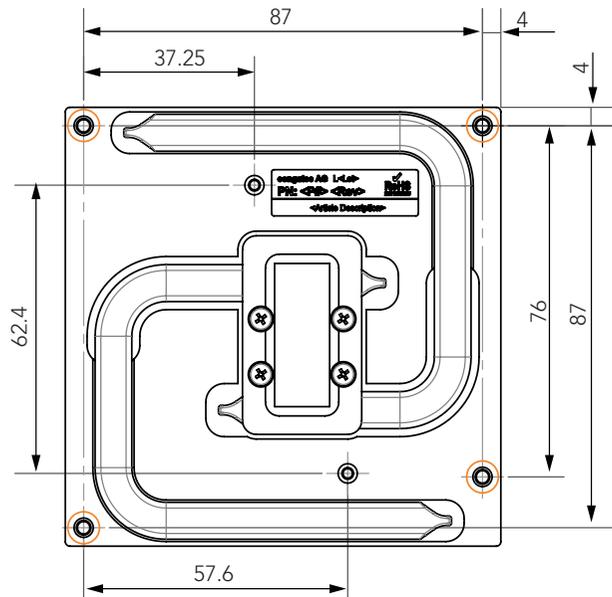
## 4.2 CSP Dimensions



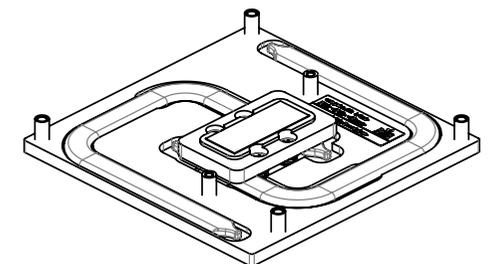
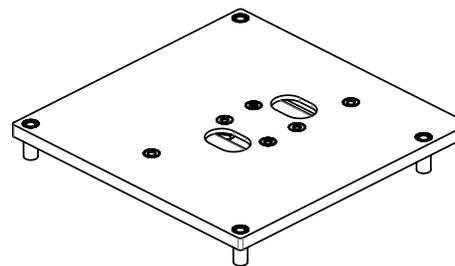
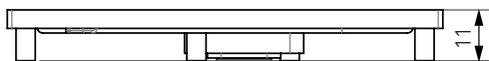
- 
 M2.5 x 11 mm threaded standoff for threaded version or
- 
 ø2.7 x 11 mm non-threaded standoff for borehole version



## 4.3 HSP Dimensions

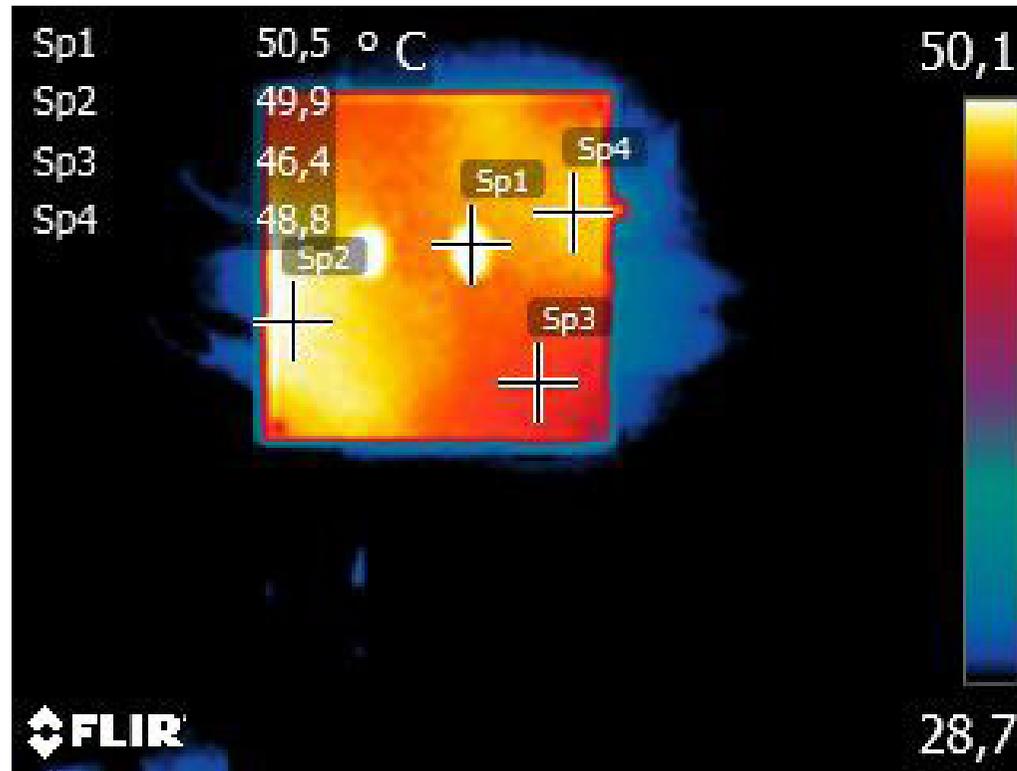


-  M2.5 x 11 mm  
 threaded standoff  
 for threaded version  
 or  
 ø2.7 x 11 mm  
 non-threaded standoff  
 for borehole version



### 4.3.2.1 Heatspreader Thermal Imagery

The conga-TC570 heatspreader solution features heatstack, heat pipe and aluminium alloy plate. The aluminium alloy plate distributes the heat evenly on the heatspreader as shown in the thermal imagery below.



## 5 Connector Rows

The conga-TC570 is connected to the carrier board via two 220-pin connectors (COM Express Type 6 pinout). These connectors are broken down into four rows. The primary connector consists of rows A and B while the secondary connector consists of rows C and D.

### 5.1 Primary and Secondary Connector Rows

The following subsystems can be found on the primary and secondary connector rows.

#### 5.1.1 PCI Express™

The conga-TC570 offers up to eight PCIe lanes—up to six lanes on the A–B connector and up to two lanes on the C–D connector. The conga-TC570 supports the following:

- up to 8 GTps (Gen 3) speed
- a 6x1 link default configuration (with SATA ports enabled) <sup>1,2,3</sup>.
- a 1 x4 + 2 x1 link or 2 x2 + 2 x1 link or 1 x2 + 4 x1 link via a special/customized BIOS firmware
- lane polarity inversion



#### Note

- <sup>1</sup> PCIe lane 5 and PCIe lane 6 are multiplexed with SATA port 1 and SATA port 0 respectively.
- <sup>2</sup> PCIe lane 7 is multiplexed with USB 3.2 Gen 2x1, port 3.
- <sup>3</sup> The number of PCIe lanes increases if the multiplexed ports are not enabled.

#### 5.1.2 PCI Express Graphics (PEG)

The conga-TC570 supports one PCIe x4 Gen 4 (PEG) port on the C–D connector. The port supports both graphics and storage devices and can be operated as x1 or x4 link.



#### Note

*The PEG lanes can not be linked together with the PCI Express lanes in section 5.1.1 "PCI Express™".*

## 5.1.3 Display Interfaces

The conga-TC570 offers the following display interfaces:

- three DP++
- dual-channel LVDS
- one VGA on commercial variants
- optional VGA on industrial variants
- four independent displays (DP++, eDP/LVDS and VGA)

The table below shows the supported display combinations and resolutions.

Table 10 Display Combination and Resolution

	Display 1 (DDI1)		Display 2 (DDI2)		Display 3 (DDI3)		Graphic 4	
	Interface	Max. Resolution	Interface	Max. Resolution	Interface	Max. Resolution	Interface	Graphics
Option 1	DP++	4096x2304 @ 60 Hz, 36 bpp	DP++	4096x2304 @ 60 Hz, 36 bpp	DP++	4096x2304 @ 60 Hz, 36 bpp	LVDS or eDP	1920x1200 @ 60 Hz (dual LVDS mode) 4096x2304 @ 60 Hz, 24 bpp
Option 2	DP++	4096x2304 @ 60 Hz, 36 bpp	DP++	4096x2304 @ 60 Hz, 36 bpp	DP++	4096x2304 @ 60 Hz, 36 bpp	VGA	1920x1200 @ 60 Hz
Option 3	DP++	4096x2304 @ 60 Hz, 36 bpp	DP++	4096x2304 @ 60 Hz, 36 bpp	VGA	1920x1200 @ 60 Hz	LVDS or eDP	1920x1200 @ 60 Hz (dual LVDS mode) 4096x2304 @ 60 Hz, 24 bpp



### Note

A single DP/eDP display supports maximum resolution of 5120x3200 @ 60 Hz.

### 5.1.3.1 DP++

The conga-TC570 offers three DP++ interfaces. The interfaces support:

- three independent DP displays (DP++)
- VESA DisplayPort Standard 1.2
- data rate of 1.62 GT/s, 2.97 GT/s and 5.4 GT/s on 1, 2 or 4 data lanes
- up to 4096x2304 resolutions at 60 Hz
- Audio formats such as AC-3 Dolby Digital, Dolby Digital Plus, DTS-HD, LPCM, 192 KHz/24 bit, 8 channel, Dolby TrueHD, DTS-HD Master Audio (Lossless Blu-Ray Disc Audio Format)

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### 5.1.3.2 LVDS/eDP

The conga-TC570 offers an LVDS/eDP interface. This interface is configured in the BIOS to support LVDS by default. For eDP support, go to Advanced -> Graphics -> Active LFP Configuration in the BIOS setup menu and select "eDP".

The LVDS <sup>1</sup> interface supports:

- single or dual channel LVDS (color depths of 18 bpp or 24 bpp)
- integrated flat panel interface with clock frequency up to 112 MHz
- VESA and OpenLDI LVDS color mappings
- automatic panel detection via Embedded Panel Interface based on VESA EDID™ 1.3
- resolution up to 1920x1200 in dual LVDS channel mode

The eDP <sup>1,2</sup> interface supports:

- eDP 1.4 specification
- Spread-Spectrum Clocking
- eDP display authentication



#### Note

<sup>1.</sup> The LVDS/eDP interface does not support both LVDS and eDP signals at the same time.

<sup>2.</sup> The eDP interface does not support HDCP

### 5.1.3.3 VGA

The Intel® Tiger Lake IoT UP3 SoC does not natively support VGA interface. However, the conga-TC570 commercial variants support this interface by integrating a DisplayPort to VGA adapter chip.



#### Note

*For VGA support on industrial variants, you need a customized conga-TC570 variant.*

## 5.1.4 SATA

The conga-TC570 offers two SATA interfaces (SATA 0-1) on the A–B connector. The interfaces support:

- independent DMA operation
- data transfer rates up to 6.0 Gb/s
- AHCI mode using memory space and RAID mode
- Hot-plug detect



### Note

1. *SATA0 is multiplexed with PCIe6 while SATA1 is multiplexed with PCIe5.*
2. *The interface does not support legacy mode using I/O space.*

## 5.1.5 USB

The conga-TC570 offers eight USB 2.0 interfaces on the A–B connector and up to four SuperSpeed signals on the C–D connector. The xHCI host controller supports:

- USB 3.2 specification
- SuperSpeedPlus, SuperSpeed, High-Speed, Full-Speed and Low-Speed USB signaling
- data transfers of up to 10 Gbps for USB 3.2 Gen 2x1 port
- data transfers of up to 5 Gbps for USB 3.2 Gen 1x1 port
- supports USB debug port on all USB 3.2 capable ports



### Note

1. *The USB 3.2 Gen 2x1, port 3 is multiplexed with PCIe7.*
2. *The USB ports are configured in the BIOS setup menu to operate by default in Gen 1 mode. Before you change the default setting to Gen 2, ensure the carrier board is designed for Gen 2 operation. For Gen 2 design considerations, contact congatec technical support center.*

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## 5.1.6 Gigabit Ethernet

The conga-TC570 offers a 2.5 Gigabit Ethernet interface via an onboard Intel® i225LM/V/IT Phy. The interface supports:

- full-duplex operation at 10/100/1000/2500 Mbps <sup>1,2</sup>
- half-duplex operation at 10/100 Mbps <sup>1,2</sup>
- Time Sensitive Networking <sup>3,4</sup>



### Note

- <sup>1</sup> The GBE0\_LINK# output is not active during a 10 Mb connection. It is only active during a 100 Mb or 1 Gb connection. This is a limitation of Ethernet Phy since it has only three LED outputs—ACT#, LINK100# and LINK1000#.
- <sup>2</sup> The GBE0\_LINK# signal is a logic AND of the GBE0\_LINK100# and GBE0\_LINK1000# signals on the conga-TC570 module.
- <sup>3</sup> For real time applications, we recommend to use conga-TC570 industrial variants for Intel® TCC/TSN feature.
- <sup>4</sup> Not supported in Windows Operating Systems

## 5.1.7 High Definition Audio

The conga-TC570 provides an HD audio interface on the A–B connector.

## 5.1.8 LPC Bus

The conga-TC570 offers the LPC bus through an eSPI to LPC bridge. For information about the decoded LPC addresses, see section 9.1.1 “LPC Bus”.

## 5.1.9 I<sup>2</sup>C Bus

The I<sup>2</sup>C bus is implemented through the congatec board controller and accessed through the congatec CGOS driver and API. The controller provides a fast-mode multi-master I<sup>2</sup>C bus that has the maximum I<sup>2</sup>C bandwidth.

## 5.1.10 GPIOs

The conga-TC570 offers General Purpose Input/Output signals on the A–B connector. The GPIO signals are controlled by the congatec Board controller.

## 5.1.11 General Purpose Serial Interface

The conga-TC570 offers two standard 16C550 UARTs on the A–B connector via the congatec Board Controller. The interfaces support up to 115200 baud rate.



### Note

*The UART interfaces do not support hardware handshake and flow control.*

## 5.1.12 Power Control

### PWR\_OK

Power OK from main power supply or carrier board voltage regulator circuitry. A high value indicates that the power is good and the module can start its onboard power sequencing.

Carrier board hardware must drive this signal low until all power rails and clocks are stable. Releasing PWR\_OK too early or not driving it low at all can cause numerous boot up problems. It is a good design practice to delay the PWR\_OK signal a little (typically 100ms) after all carrier board power rails are up, to ensure a stable system.

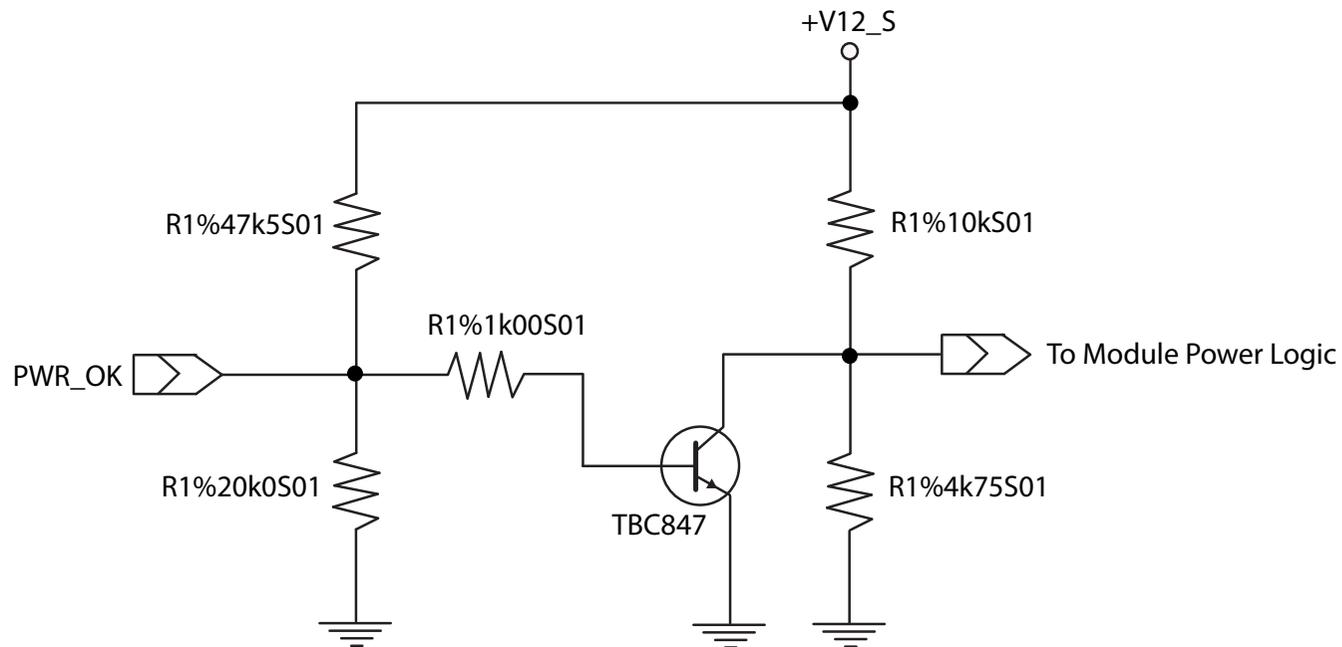
A sample screenshot is shown below:



### Note

*The module is kept in reset as long as the PWR\_OK is driven by carrier board hardware.*

The conga-TC570 PWR\_OK input circuitry is implemented as shown below:



The voltage divider ensures that the input complies with 3.3 V CMOS characteristic and also makes it possible to use the module on carrier board designs that do not drive the PWR\_OK signal. Although the PWR\_OK input is not mandatory for the onboard power-up sequencing, it is strongly recommended that the carrier board hardware drives the signal low until it is safe to let the module boot-up.

When considering the above shown voltage divider circuitry and the transistor stage, the voltage measured at the PWR\_OK input pin may be only around 0.8 V when the 12 V is applied to the module. Actively driving PWR\_OK high is compliant to the COM Express specification but this can cause back driving. Therefore, congatec recommends driving the PWR\_OK low to keep the module in reset and tri-state PWR\_OK when the carrier board hardware is ready to boot.

The three typical usage scenarios for a carrier board design are:

- Connect PWR\_OK to the “power good” signal of an ATX type power supply.
- Connect PWR\_OK to the last voltage regulator in the chain on the carrier board.
- Simply pull PWR\_OK with a 1k resistor to the carrier board 3.3 V power rail.

With this solution, you must ensure that by the time the 3.3 V is up, all carrier board hardware is fully powered and all clocks are stable.

---

The conga-TC570 supports the controlling of ATX-style power supplies. If you do not use an ATX power supply, do not connect the conga-TC570 pins SUS\_S3/PS\_ON, 5V\_SB, and PWRBTN#.

### **SUS\_S3#/PS\_ON#**

The SUS\_S3#/PS\_ON# (pin A15 on the A–B connector) signal is an active-low output that can be used to turn on the main outputs of an ATX-style power supply. To accomplish this the signal must be inverted with an inverter/transistor that is supplied by standby voltage and is located on the carrier board.

### **PWRBTN#**

When using ATX-style power supplies, PWRBTN# (pin B12 on the A–B connector) is used to connect to a momentary-contact, active-low debounced push-button input while the other terminal on the push-button must be connected to ground. This signal is internally pulled up to 3V\_SB using a 100 kΩ resistor. When PWRBTN# is asserted it indicates that an operator wants to turn the power on or off. The response to this signal from the system may vary as a result of modifications made in BIOS settings or by system software.

## Standard 12V Power Supply Implementation Guidelines

The 12 volt input power is the sole operational power source for the conga-TC570. Other required voltages are generated internally on the module using onboard voltage regulators.



*When designing a power supply for a conga-TC570 application, be aware that the system may malfunction when a 12V power supply that produces non-monotonic voltage is used to power the system up. Though this problem is rare, it has been observed in some mobile power supply applications.*

*The cause of this problem is that some internal circuits on the module (e.g. clock-generator chips) generate their own reset signals when the supply voltage exceeds a certain voltage threshold. A voltage dip after passing this threshold may lead to these circuits becoming confused, thereby resulting in a malfunction.*

*To ensure this problem does not occur, observe the power supply rise waveform through an oscilloscope, during the power supply qualification phase. This will help to determine if the rise is indeed monotonic and does not have any dips. For more information, see the “Power Supply Design Guide for Desktop Platform Form Factors” document at [www.intel.com](http://www.intel.com).*

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## 5.1.13 Power Management

### ACPI

The conga-TC570 supports Advanced Configuration and Power Interface (ACPI) specification, revision 4.0a. It also supports Suspend to RAM (S3). For more information, see section 7.5 “ACPI Suspend Modes and Resume Events”.

### DEEP Sx

The Deep Sx is a lower power state employed to minimize the power consumption while in S3/S4/S5. In the Deep Sx state, the system entry condition determines if the system context is maintained or not. All power is shut off except for minimal logic which supports limited set of wake events for Deep Sx. The Deep Sx on resumption, puts system back into the state it is entered from. In other words, if Deep Sx state was entered from S3 state, then the resume path will place system back into S3.

### S5e Power State

The conga-TC570 features a congatec proprietary Enhanced Soft-Off power state. See section 6.1.7 “Enhanced Soft-Off State” for more information.

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## 6 Additional Features

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The following features are available on the conga-TC570.

### 6.1 congatec Board Controller (cBC)

The conga-TC570 is equipped with Microchip microcontroller. This onboard microcontroller plays an important role for most of the congatec embedded/industrial PC features. It fully isolates some of the embedded features such as system monitoring or the I<sup>2</sup>C bus from the x86 core architecture, which results in higher embedded feature performance and more reliability, even when the x86 processor is in a low power mode. It also ensures that the congatec embedded feature set is fully compatible amongst all congatec modules.

The board controller supports the following features:

#### 6.1.1 Board Information

The cBC provides a rich data-set of manufacturing and board information such as serial number, EAN number, hardware and firmware revisions, and so on. It also keeps track of dynamically changing data like runtime meter and boot counter.

#### 6.1.2 General Purpose Input/Output

The conga-TC570 offers general purpose inputs and outputs for custom system design. These GPIOs are controlled by the cBC.

#### 6.1.3 Watchdog

The conga-TC570 is equipped with a multi stage watchdog solution that is triggered by software. For more information about the Watchdog feature, see the application note AN3\_Watchdog.pdf on the congatec GmbH website at [www.congatec.com](http://www.congatec.com).



*The conga-TC570 module does not support the watchdog NMI mode.*

#### 6.1.4 I<sup>2</sup>C Bus

The conga-TC570 supports I<sup>2</sup>C bus. Thanks to the I<sup>2</sup>C host controller in the cBC, the I<sup>2</sup>C bus is multi-master capable and runs at fast mode.

---

## 6.1.5 Power Loss Control

The cBC has full control of the power-up of the module and therefore can be used to specify the behavior of the system after an AC power loss condition. Supported modes are “Always On”, “Remain Off” and “Last State”.

## 6.1.6 Fan Control

The conga-TC570 has additional signals and functions to further improve system management. One of these signals is FAN\_PWMOUT, an output signal that allows system fan control using a PWM (Pulse Width Modulation) output. Additionally, there is an input signal called FAN\_TACHOIN that provides the ability to monitor the system’s fan RPMs (revolutions per minute). This signal must receive two pulses per revolution in order to produce an accurate reading. For this reason, a two pulse per revolution fan or similar hardware solution is recommended.



### Note

1. A four wire fan must be used to generate the correct speed readout.
2. For the correct fan control (FAN\_PWMOUT, FAN\_TACHIN) implementation, see the COM Express Design Guide.

## 6.1.7 Enhanced Soft-Off State

The conga-TC570 supports an enhanced Soft-Off state (S5e)—a congatec proprietary low-power Soft-Off state. In this state, the CPU module switches off almost all the onboard logic in order to reduce the power consumption to absolute minimum (between 0.05 mA and 0.09 mA).

Refer to congatec application note AN36\_Enhanced\_Soft\_Off.pdf for detailed description of the S5e state.

## 6.2 OEM BIOS Customization

The conga-TC570 is equipped with congatec Embedded BIOS, which is based on American Megatrends Inc. Aptio UEFI firmware. The congatec Embedded BIOS allows system designers to modify the BIOS. For more information about customizing the congatec Embedded BIOS, refer to the congatec System Utility user’s guide CGUTLm1x.pdf on the congatec website at [www.congatec.com](http://www.congatec.com) or contact technical support.

The customization features supported are described below:

---

## 6.2.1 OEM Default Settings

This feature allows system designers to create and store their own BIOS default configuration. Customized BIOS development by congatec for OEM default settings is no longer necessary because customers can easily perform this configuration by themselves using the congatec system utility CGUTIL. See congatec application note AN8\_Create\_OEM\_Default\_Map.pdf on the congatec website for details on how to add OEM default settings to the congatec Embedded BIOS.

## 6.2.2 OEM Boot Logo

This feature allows system designers to replace the standard text output displayed during POST with their own BIOS boot logo. Customized BIOS development by congatec for OEM Boot Logo is no longer necessary because customers can easily perform this configuration by themselves using the congatec system utility CGUTIL. See congatec application note AN8\_Create\_And\_Add\_Bootlogo.pdf on the congatec website for details on how to add OEM boot logo to the congatec Embedded BIOS.

## 6.2.3 OEM POST Logo

This feature allows system designers to replace the congatec POST logo displayed in the upper left corner of the screen during BIOS POST with their own BIOS POST logo. Use the congatec system utility CGUTIL 1.5.4 or later to replace/add the OEM POST logo.

## 6.2.4 OEM BIOS Code/Data

With the congatec embedded BIOS it is possible for system designers to add their own code to the BIOS POST process. The congatec Embedded BIOS first calls the OEM code before handing over control to the OS loader.

Except for custom specific code, this feature can also be used to support verb tables for HDA codecs, PCI/PCIe OpROMs, bootloaders, rare graphic modes and Super I/O controller initialization.



*The OEM BIOS code of the new UEFI based firmware is only called when the CSM (Compatibility Support Module) is enabled in the BIOS setup menu. Contact congatec technical support for more information on how to add OEM code.*

## 6.2.5 OEM DXE Driver

This feature allows designers to add their own UEFI DXE driver to the congatec embedded BIOS. Contact congatec technical support for more information on how to add an OEM DXE driver.

---

## 6.3 congatec Battery Management Interface

To facilitate the development of battery powered mobile systems based on embedded modules, congatec GmbH defined an interface for the exchange of data between a CPU module (using an ACPI operating system) and a Smart Battery system. A system developed according to the congatec Battery Management Interface Specification can provide the battery management functions supported by an ACPI capable operating system (for example, charge state of the battery, information about the battery, alarms/events for certain battery states and so on) without the need for additional modifications to the system BIOS.

In addition to the ACPI-Compliant Control Method Battery mentioned above, the latest versions of the conga-TC570 BIOS and board controller firmware also support LTC1760 battery manager from Linear Technology and a battery only solution (no charger). All three battery solutions are supported on the I2C bus and the SMBus. This gives the system designer more flexibility when choosing the appropriate battery sub-system.

For more information about the supported Battery Management Interface, contact your local sales representative.

## 6.4 API Support (CGOS)

In order to benefit from the above mentioned non-industry standard feature set, congatec provides an API that allows application software developers to easily integrate all these features into their code. The CGOS API (congatec Operating System Application Programming Interface) is the congatec proprietary API that is available for all commonly used Operating Systems such as Win32, Win64, Win CE, Linux. The architecture of the CGOS API driver provides the ability to write application software that runs unmodified on all congatec CPU modules. All the hardware related code is contained within the congatec embedded BIOS on the module. See section 1.1 of the CGOS API software developers guide, available on the congatec website.

## 6.5 Security Features

The conga-TC570 offers a discrete SPI TPM 2.0 (Infineon SLB9670VQ2.0) by default.

## 6.6 Suspend to Ram

The Suspend to RAM feature is available on the conga-TC570.

# 7 conga Tech Notes

The conga-TC570 has some technological features that require additional explanation. The following section will give the reader a better understanding of some of these features.

## 7.1 Adaptive Thermal Monitor and Catastrophic Thermal Protection

Intel® Xeon, Core™ i7/i5/i3 and Celeron® and Pentium® processors have a thermal monitor feature that helps to control the processor temperature. The integrated TCC (Thermal Control Circuit) activates if the processor silicon reaches its maximum operating temperature. The activation temperature that the Intel® Thermal Monitor uses to activate the TCC can be slightly modified via TCC Activation Offset in BIOS setup submenu "CPU submenu".

The Adaptive Thermal Monitor controls the processor temperature using two methods:

- Adjusting the processor's operating frequency and core voltage (EIST transitions)
- Modulating (start/stop) the processor's internal clocks at a duty cycle of 25% on and 75% off

When activated, the TCC causes both processor core and graphics core to reduce frequency and voltage adaptively. The Adaptive Thermal Monitor will remain active as long as the package temperature remains at its specified limit. Therefore, the Adaptive Thermal Monitor will continue to reduce the package frequency and voltage until the TCC is de-activated. Clock modulation is activated if frequency and voltage adjustments are insufficient. Additional hardware, software driver, or operating system support is not required.

Intel®'s Core™ i7/i5/i3, Celeron® and Pentium® processors use the THERMTRIP# signal to shut down the system if the processor's silicon reaches a temperature of approximately 125°C. The THERMTRIP# signal activation is completely independent from processor activity and therefore does not produce any bus cycles.



- Note**
1. For THERMTRIP# to switch off the system automatically, use an ATX style power supply
  2. The maximum operating temperature for Intel® Core™ i7/i5/i3, Celeron® and Pentium® processors is 100°C
  3. To ensure that the TCC is active for only short periods of time, thus reducing the impact on processor performance to a minimum, it is necessary to have a properly designed thermal solution. The Intel® Core™ i7/i5/i3, Celeron® and Pentium® processor's respective datasheet can provide you with more information about this subject.

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## 7.2 Processor Performance Control

### 7.2.1 Intel® SpeedStep® Technology (EIST)

Intel® processors found on the conga-TC570 run at different voltage/frequency states (performance states), which is referred to as Enhanced Intel® SpeedStep® Technology (EIST). Operating systems that support performance control take advantage of microprocessors that use several different performance states in order to efficiently operate the processor when it is not being fully used. The operating system will determine the necessary performance state that the processor should run at so that the optimal balance between performance and power consumption can be achieved during runtime. The Windows family of operating systems links its processor performance control policy to the power scheme setting. You must ensure that the power scheme setting you choose has the ability to support Enhanced Intel® SpeedStep® technology.

The 11th Generation Intel® Core™ processor family supports Intel Speed Shift, a new and energy efficient method for frequency control. This feature is also referred to as Hardware-controlled Performance States (HWP). It is a hardware implementation of the ACPI defined Collaborative Processor Performance Control (CPPC2) and is supported by newer operating systems (Win 8.1 or newer).

With this feature enabled, the processor autonomously selects performance states based on workload demand and thermal limits while also considering information provided by the OS e.g., the performance limits and workload history.

### 7.2.2 Intel® Turbo Boost Technology

Intel® Turbo Boost Technology allows processor cores to run faster than the base operating frequency if it is operating below power, current, and temperature specification limits. Intel® Turbo Boost Technology is activated when the Operating System (OS) requests the highest processor performance state. The maximum frequency of Intel® Turbo Boost Technology depends on the number of active cores. The amount of time the processor spends in the Intel Turbo Boost Technology state depends on the workload and operating environment.

Any of the following can set the upper limit of Intel® Turbo Boost Technology on a given workload:

- Number of active cores
- Estimated current consumption
- Estimated power consumption
- Processor temperature

When the processor is operating below these limits and the user's workload demands additional performance, the processor frequency dynamically increases by 100 MHz on short and regular intervals until the upper limit is met or the maximum possible upside for the number of active cores is reached. For more information about Intel® Turbo Boost Technology, visit the Intel® website.



## Note

1. Only conga-TC570 variants that feature the Core™ i7, i5 and i3 processors support Intel® Turbo Boost Technology. Refer to section 1.2 “Options Information” for information about the maximum turbo frequency available for conga-TC570 variants.
2. For real-time sensitive applications, disable EIST and Turbo Mode in the BIOS setup to ensure a more deterministic performance.
3. Disable Turbo mode for industrial use condition applications.

## 7.3 Intel® Virtualization Technology

Intel® Virtualization Technology (Intel® VT) makes a single system appear as multiple independent systems to software. With this technology, multiple, independent operating systems can run simultaneously on a single system. The technology components support virtualization of platforms based on Intel architecture microprocessors and chipsets. Intel® Virtualization Technology for IA-32, Intel® 64 and Intel® Architecture (Intel® VT-x) added hardware support in the processor to improve the virtualization performance and robustness.

RTS Real-Time Hypervisor supports Intel VT and is verified on all current congatec x86 hardware.



## Note

congatec supports RTS Hypervisor.

## 7.4 Thermal Management

ACPI is responsible for allowing the operating system to play an important part in the system’s thermal management. This results in the operating system having the ability to implement cooling decisions according to the demands of the application.

The conga-TC570 offers hardware-based support for passive and active cooling. Passive cooling is implemented in the Intel CPU via the Thermal Control Circuit (TCC ) Activation Offset setting in the CPU configuration setup sub-menu. The TCC in the processor is activated at 100°C by default but can be lowered by the Activation Offset—for example, an activation offset of “10” will activate TCC at 90°C. ACPI OS support is not required. See section 7.1 “Adaptive Thermal Monitor and Catastrophic Thermal Protection” for more information.

The congatec board controller supports active cooling solution. The board controller controls the fan’s speed based on the temperature readings of the CPU. This feature does not require ACPI OS support. The only software-controlled thermal trip point on conga-TC570 is the Critical Trip Point. The active or passive cooling policy should ensure that the CPU temperature does not reach this trip point. However, if the critical trip point is reached, the OS will shut down properly in order to prevent damage to the system.

Use the “critical trip point” setup node in the BIOS setup menu to determine the temperature threshold at which the system shuts down.



## Note

The Automatic Critical Trip Point BIOS setting shuts down the system at 5°C above the maximum specified temperature of the processor

## 7.5 ACPI Suspend Modes and Resume Events

The conga-TC570 BIOS supports S3 (Suspend to RAM), S4 (Suspend to Disk) and S5 (Soft-Off).

**Table 11** Wake Events

The table below lists the events that wake the system from S3-S5.

Wake Event	Conditions/Remarks
Power Button	Wakes unconditionally from S3-S5.
Onboard LAN Event	Device driver must be configured for Wake On LAN support.
SMBALERT#	Wakes unconditionally from S3-S5.
PCI Express WAKE#	Wakes unconditionally from S3-S5.
WAKE#	Wakes unconditionally from S3.
PME#	Activate the wake up capabilities of a PCI device using Windows Device Manager configuration options for this device OR set Resume On PME# to Enabled in the Power setup menu.
USB Mouse/Keyboard Event	When Standby mode is set to S3, USB hardware must be powered by standby power source. Set USB Device Wakeup from S3/S4 to ENABLED in the ACPI setup menu (if setup node is available in BIOS setup program). In Device Manager look for the keyboard/mouse devices. Go to the Power Management tab and check 'Allow this device to bring the computer out of standby'.
RTC Alarm	Activate and configure Resume On RTC Alarm in the Power setup menu. Only available in S5.
Watchdog Power Button Event	Wakes unconditionally from S3-S5.

## 8 Signal Descriptions and Pinout Tables

The following section describes the signals found on COM Express™ Type 6 connectors used for congatec GmbH modules. The pinout of the modules complies with COM Express Type 6, rev. 3.0.

The table below describes the terminology used in this section. The PU/PD column indicates if a pull-up or pull-down resistor has been used. If the field entry area in this column for the signal is empty, then no pull-up or pull-down resistor has been implemented by congatec.

The “#” symbol at the end of the signal name indicates that the active or asserted state occurs when the signal is at a low voltage level. When “#” is not present, the signal is asserted when at a high voltage level.

Table 12 Signal Tables Terminology Descriptions

Term	Description
PU	Implemented pull-up resistor
PD	Implemented pull-down resistor
I/O 3.3V	Bi-directional signal 3.3V tolerant
I/O 5V	Bi-directional signal 5V tolerant
I 3.3V	Input 3.3V tolerant
I 5V	Input 5V tolerant
I/O 3.3VSB	Input or output 3.3V tolerant active in standby state
O 3.3V	Output 3.3V signal level
O 5V	Output 5V signal level
OD	Open drain output
P	Power Input/Output
DDC	Display Data Channel
PCIE	PCI Express compatible differential signal. In compliance with PCI Express Specification.
PEG	PCI Express Graphics
SATA	In compliance with Serial ATA specification Revision 2.6 and 3.0.
LVDS	Low Voltage Differential Signal - 330 mV nominal; 450 mV maximum differential signal
REF	Reference voltage output. May be sourced from a module power plane.
PDS	Pull-down strap. A module output pin that is either tied to GND or is not connected. Used to signal module capabilities (pinout type) to the Carrier Board.

## 8.1 Connector Signal Descriptions

Table 13 Connector A–B Pinout

Pin	Row A	Pin	Row B	Pin	Row A	Pin	Row B
A1	GND (FIXED)	B1	GND (FIXED)	A56	PCIE_TX4-	B56	PCIE_RX4-
A2	GBE0_MDI3-	B2	GBE0_ACT#	A57	GND	B57	GPO2
A3	GBE0_MDI3+	B3	LPC_FRAME#/ESPI_CS0#	A58	PCIE_TX3+	B58	PCIE_RX3+
A4	GBE0_LINK100#	B4	LPC_AD0/ESPI_IO_0	A59	PCIE_TX3-	B59	PCIE_RX3-
A5	GBE0_LINK1000#	B5	LPC_AD1/ESPI_IO_1	A60	GND (FIXED)	B60	GND (FIXED)
A6	GBE0_MDI2-	B6	LPC_AD2/ESPI_IO_2	A61	PCIE_TX2+	B61	PCIE_RX2+
A7	GBE0_MDI2+	B7	LPC_AD3/ESPI_IO_3	A62	PCIE_TX2-	B62	PCIE_RX2-
A8	GBE0_LINK#	B8	LPC_DRQ0#/ESPI_ALERT0#	A63	GPI1	B63	GPO3
A9	GBE0_MDI1-	B9	LPC_DRQ1#/ESPI_ALERT1#	A64	PCIE_TX1+	B64	PCIE_RX1+
A10	GBE0_MDI1+	B10	LPC_CLK/ESPI_CK	A65	PCIE_TX1-	B65	PCIE_RX1-
A11	GND (FIXED)	B11	GND (FIXED)	A66	GND	B66	WAKE0#
A12	GBE0_MDI0-	B12	PWRBTN#	A67	GPI2	B67	WAKE1#
A13	GBE0_MDI0+	B13	SMB_CK	A68	PCIE_TX0+	B68	PCIE_RX0+
A14	GBE0_CTREF <sup>1</sup>	B14	SMB_DAT	A69	PCIE_TX0-	B69	PCIE_RX0-
A15	SUS_S3#	B15	SMB_ALERT# <sup>3</sup>	A70	GND (FIXED)	B70	GND (FIXED)
A16	SATA0_TX+	B16	SATA1_TX+	A71	eDP_TX2+/LVDS_A0+	B71	LVDS_B0+
A17	SATA0_TX-	B17	SATA1_TX-	A72	eDP_TX2-/LVDS_A0-	B72	LVDS_B0-
A18	SUS_S4#	B18	SUS_STAT#/ESPI_RESET#	A73	eDP_TX1+/LVDS_A1+	B73	LVDS_B1+
A19	SATA0_RX+	B19	SATA1_RX+	A74	eDP_TX1-/LVDS_A1-	B74	LVDS_B1-
A20	SATA0_RX-	B20	SATA1_RX-	A75	eDP_TX0+/LVDS_A2+	B75	LVDS_B2+
A21	GND (FIXED)	B21	GND (FIXED)	A76	eDP_TX0-/LVDS_A2-	B76	LVDS_B2-
A22	SATA2_TX+ <sup>1</sup>	B22	SATA3_TX+ <sup>1</sup>	A77	eDP_VDD_EN/LVDS_VDD_EN	B77	LVDS_B3+
A23	SATA2_TX- <sup>1</sup>	B23	SATA3_TX- <sup>1</sup>	A78	LVDS_A3+	B78	LVDS_B3-
A24	SUS_S5#	B24	PWR_OK	A79	LVDS_A3-	B79	eDP_BKLT_EN/LVDS_BKLT_EN
A25	SATA2_RX+ <sup>1</sup>	B25	SATA3_RX+ <sup>1</sup>	A80	GND (FIXED)	B80	GND (FIXED)
A26	SATA2_RX- <sup>1</sup>	B26	SATA3_RX- <sup>1</sup>	A81	eDP_TX3+/LVDS_A_CK+	B81	LVDS_B_CK+
A27	BATLOW#	B27	WDT	A82	eDP_TX3-/LVDS_A_CK-	B82	LVDS_B_CK-
A28	(S)ATA_ACT#	B28	HDA_SDIN2 <sup>1</sup>	A83	eDP_AUX+/LVDS_I2C_CK	B83	eDP/LVDS_BKLT_CTRL
A29	HDA_SYNC	B29	HDA_SDIN1	A84	eDP_AUX-/LVDS_I2C_DAT	B84	VCC_5V_SBY
A30	HDA_RST#	B30	HDA_SDIN0	A85	GPI3	B85	VCC_5V_SBY

Pin	Row A	Pin	Row B	Pin	Row A	Pin	Row B
A31	GND (FIXED)	B31	GND (FIXED)	A86	RSVD	B86	VCC_5V_SBY
A32	HDA_BITCLK	B32	SPKR <sup>3</sup>	A87	eDP_HPD	B87	VCC_5V_SBY
A33	HDA_SDOOUT <sup>3</sup>	B33	I2C_CK	A88	PCIE_CLK_REF+	B88	BIOS_DIS1# <sup>3</sup>
A34	BIOS_DIS0# <sup>3</sup> /ESPI_SAFS	B34	I2C_DAT	A89	PCIE_CLK_REF-	B89	VGA_RED
A35	THRMTRIP#	B35	THRM#	A90	GND (FIXED)	B90	GND (FIXED)
A36	USB6-	B36	USB7-	A91	SPI_POWER	B91	VGA_GRN
A37	USB6+	B37	USB7+	A92	SPI_MISO <sup>3</sup>	B92	VGA_BLU
A38	USB_6_7_OC#	B38	USB_4_5_OC#	A93	GPO0	B93	VGA_HSYNC
A39	USB4-	B39	USB5-	A94	SPI_CLK	B94	VGA_VSYNC
A40	USB4+	B40	USB5+	A95	SPI_MOSI <sup>3</sup>	B95	VGA_I2C_CK
A41	GND (FIXED)	B41	GND (FIXED)	A96	TPM_PP	B96	VGA_I2C_DAT
A42	USB2-	B42	USB3-	A97	TYPE10# <sup>1</sup>	B97	SPI_CS#
A43	USB2+	B43	USB3+	A98	SER0_TX	B98	RSVD <sup>1</sup>
A44	USB_2_3_OC#	B44	USB_0_1_OC#	A99	SER0_RX	B99	RSVD <sup>1</sup>
A45	USB0-	B45	USB1-	A100	GND (FIXED)	B100	GND (FIXED)
A46	USB0+	B46	USB1+	A101	SER1_TX	B101	FAN_PWMOUT
A47	VCC_RTC	B47	ESPI_EN# <sup>1</sup>	A102	SER1_RX	B102	FAN_TACHIN
A48	RSVD <sup>1</sup>	B48	USB0_HOST_PRSNT <sup>2</sup>	A103	LID#	B103	SLEEP#
A49	GBE0_SDP	B49	SYS_RESET#	A104	VCC_12V	B104	VCC_12V
A50	LPC_SERIRQ/ESPI_CS1#	B50	CB_RESET#	A105	VCC_12V	B105	VCC_12V
A51	GND (FIXED)	B51	GND (FIXED)	A106	VCC_12V	B106	VCC_12V
A52	PCIE_TX5+	B52	PCIE_RX5+	A107	VCC_12V	B107	VCC_12V
A53	PCIE_TX5-	B53	PCIE_RX5-	A108	VCC_12V	B108	VCC_12V
A54	GPIO	B54	GPO1	A109	VCC_12V	B109	VCC_12V
A55	PCIE_TX4+	B55	PCIE_RX4+	A110	GND (FIXED)	B110	GND (FIXED)

### Note

1. *Not connected*
2. *Not supported*
3. *Bootstrap signals*

Table 14 Connector C–D Pinout

Pin	Row C	Pin	Row D	Pin	Row C	Pin	Row D
C1	GND (FIXED)	D1	GND (FIXED)	C56	PEG_RX1-	D56	PEG_TX1-
C2	GND	D2	GND	C57	TYPE1# <sup>1</sup>	D57	TYPE2#
C3	USB_SSRX0-	D3	USB_SSTX0-	C58	PEG_RX2+	D58	PEG_TX2+
C4	USB_SSRX0+	D4	USB_SSTX0+	C59	PEG_RX2-	D59	PEG_TX2-
C5	GND	D5	GND	C60	GND (FIXED)	D60	GND (FIXED)
C6	USB_SSRX1-	D6	USB_SSTX1-	C61	PEG_RX3+	D61	PEG_TX3+
C7	USB_SSRX1+	D7	USB_SSTX1+	C62	PEG_RX3-	D62	PEG_TX3-
C8	GND	D8	GND	C63	RSVD	D63	RSVD <sup>1</sup>
C9	USB_SSRX2-	D9	USB_SSTX2-	C64	RSVD	D64	RSVD <sup>1</sup>
C10	USB_SSRX2+	D10	USB_SSTX2+	C65	PEG_RX4+ <sup>1</sup>	D65	PEG_TX4+ <sup>1</sup>
C11	GND (FIXED)	D11	GND (FIXED)	C66	PEG_RX4- <sup>1</sup>	D66	PEG_TX4- <sup>1</sup>
C12	USB_SSRX3-	D12	USB_SSTX3-	C67	RAPID_SHUTDOWN <sup>1,2</sup>	D67	GND
C13	USB_SSRX3+	D13	USB_SSTX3+	C68	PEG_RX5+ <sup>1</sup>	D68	PEG_TX5+ <sup>1</sup>
C14	GND	D14	GND	C69	PEG_RX5- <sup>1</sup>	D69	PEG_TX5- <sup>1</sup>
C15	DDI1_PAIR6+ <sup>1</sup>	D15	DDI1_CTRLCLK_AUX+	C70	GND (FIXED)	D70	GND (FIXED)
C16	DDI1_PAIR6- <sup>1</sup>	D16	DDI1_CTRLDATA_AUX- <sup>3</sup>	C71	PEG_RX6+ <sup>1</sup>	D71	PEG_TX6+ <sup>1</sup>
C17	RSVD	D17	RSVD	C72	PEG_RX6- <sup>1</sup>	D72	PEG_TX6- <sup>1</sup>
C18	RSVD	D18	RSVD	C73	GND	D73	GND
C19	PCIE_RX6+	D19	PCIE_TX6+	C74	PEG_RX7+ <sup>1</sup>	D74	PEG_TX7+ <sup>1</sup>
C20	PCIE_RX6-	D20	PCIE_TX6-	C75	PEG_RX7- <sup>1</sup>	D75	PEG_TX7- <sup>1</sup>
C21	GND (FIXED)	D21	GND (FIXED)	C76	GND	D76	GND
C22	PCIE_RX7+	D22	PCIE_TX7+	C77	RSVD <sup>1</sup>	D77	RSVD <sup>1</sup>
C23	PCIE_RX7-	D23	PCIE_TX7-	C78	PEG_RX8+ <sup>1</sup>	D78	PEG_TX8+ <sup>1</sup>
C24	DDI1_HPD	D24	RSVD	C79	PEG_RX8- <sup>1</sup>	D79	PEG_TX8- <sup>1</sup>
C25	DDI1_PAIR4+ <sup>1</sup>	D25	RSVD	C80	GND (FIXED)	D80	GND (FIXED)
C26	DDI1_PAIR4- <sup>1</sup>	D26	DDI1_PAIR0+	C81	PEG_RX9+ <sup>1</sup>	D81	PEG_TX9+ <sup>1</sup>
C27	RSVD	D27	DDI1_PAIR0-	C82	PEG_RX9- <sup>1</sup>	D82	PEG_TX9- <sup>1</sup>
C28	RSVD	D28	RSVD <sup>1</sup>	C83	RSVD <sup>1</sup>	D83	RSVD <sup>1</sup>
C29	DDI1_PAIR5+ <sup>1</sup>	D29	DDI1_PAIR1+	C84	GND	D84	GND
C30	DDI1_PAIR5- <sup>1</sup>	D30	DDI1_PAIR1-	C85	PEG_RX10+ <sup>1</sup>	D85	PEG_TX10+ <sup>1</sup>
C31	GND (FIXED)	D31	GND (FIXED)	C86	PEG_RX10- <sup>1</sup>	D86	PEG_TX10- <sup>1</sup>
C32	DDI2_CTRLCLK_AUX+	D32	DDI1_PAIR2+	C87	GND	D87	GND

Pin	Row C	Pin	Row D	Pin	Row C	Pin	Row D
C33	DDI2_CTRLDATA_AUX- <sup>3</sup>	D33	DDI1_PAIR2-	C88	PEG_RX11+ <sup>1</sup>	D88	PEG_TX11+ <sup>1</sup>
C34	DDI2_DDC_AUX_SEL	D34	DDI1_DDC_AUX_SEL	C89	PEG_RX11- <sup>1</sup>	D89	PEG_TX11- <sup>1</sup>
C35	RSVD <sup>1</sup>	D35	RSVD <sup>1</sup>	C90	GND (FIXED)	D90	GND (FIXED)
C36	DDI3_CTRLCLK_AUX+	D36	DDI1_PAIR3+	C91	PEG_RX12+ <sup>1</sup>	D91	PEG_TX12+ <sup>1</sup>
C37	DDI3_CTRLDATA_AUX- <sup>3</sup>	D37	DDI1_PAIR3-	C92	PEG_RX12- <sup>1</sup>	D92	PEG_TX12- <sup>1</sup>
C38	DDI3_DDC_AUX_SEL	D38	RSVD <sup>1</sup>	C93	GND	D93	GND
C39	DDI3_PAIR0+	D39	DDI2_PAIR0+	C94	PEG_RX13+ <sup>1</sup>	D94	PEG_TX13+ <sup>1</sup>
C40	DDI3_PAIR0-	D40	DDI2_PAIR0-	C95	PEG_RX13- <sup>1</sup>	D95	PEG_TX13- <sup>1</sup>
C41	GND (FIXED)	D41	GND (FIXED)	C96	GND	D96	GND
C42	DDI3_PAIR1+	D42	DDI2_PAIR1+	C97	RVSD <sup>1</sup>	D97	RSVD <sup>1</sup>
C43	DDI3_PAIR1-	D43	DDI2_PAIR1-	C98	PEG_RX14+ <sup>1</sup>	D98	PEG_TX14+ <sup>1</sup>
C44	DDI3_HPD	D44	DDI2_HPD	C99	PEG_RX14- <sup>1</sup>	D99	PEG_TX14- <sup>1</sup>
C45	RSVD <sup>1</sup>	D45	RSVD <sup>1</sup>	C100	GND (FIXED)	D100	GND (FIXED)
C46	DDI3_PAIR2+	D46	DDI2_PAIR2+	C101	PEG_RX15+ <sup>1</sup>	D101	PEG_TX15+ <sup>1</sup>
C47	DDI3_PAIR2-	D47	DDI2_PAIR2-	C102	PEG_RX15- <sup>1</sup>	D102	PEG_TX15- <sup>1</sup>
C48	RSVD <sup>1</sup>	D48	RSVD <sup>1</sup>	C103	GND	D103	GND
C49	DDI3_PAIR3+	D49	DDI2_PAIR3+	C104	VCC_12V	D104	VCC_12V
C50	DDI3_PAIR3-	D50	DDI2_PAIR3-	C105	VCC_12V	D105	VCC_12V
C51	GND (FIXED)	D51	GND (FIXED)	C106	VCC_12V	D106	VCC_12V
C52	PEG_RX0+	D52	PEG_TX0+	C107	VCC_12V	D107	VCC_12V
C53	PEG_RX0-	D53	PEG_TX0-	C108	VCC_12V	D108	VCC_12V
C54	TYPE0# <sup>1</sup>	D54	PEG_LANE_RV#	C109	VCC_12V	D109	VCC_12V
C55	PEG_RX1+	D55	PEG_TX1+	C110	GND (FIXED)	D110	GND (FIXED)

### Note

- <sup>1</sup>. Not connected
- <sup>2</sup>. Not supported
- <sup>3</sup>. Bootstrap signals

Table 15 PCI Express Signal Descriptions (General Purpose)

Signal	Pin #	Description	I/O	PU/PD	Comment
PCIE_RX0+ PCIE_RX0-	B68 B69	PCI Express channel 0, Receive Input differential pair	I PCIE		
PCIE_TX0+ PCIE_TX0-	A68 A69	PCI Express channel 0, Transmit Output differential pair	O PCIE		
PCIE_RX1+ PCIE_RX1-	B64 B65	PCI Express channel 1, Receive Input differential pair	I PCIE		
PCIE_TX1+ PCIE_TX1-	A64 A65	PCI Express channel 1, Transmit Output differential pair	O PCIE		
PCIE_RX2+ PCIE_RX2-	B61 B62	PCI Express channel 2, Receive Input differential pair	I PCIE		
PCIE_TX2+ PCIE_TX2-	A61 A62	PCI Express channel 2, Transmit Output differential pair	O PCIE		
PCIE_RX3+ PCIE_RX3-	B58 B59	PCI Express channel 3, Receive Input differential pair	I PCIE		
PCIE_TX3+ PCIE_TX3-	A58 A59	PCI Express channel 3, Transmit Output differential pair	O PCIE		
PCIE_RX4+ PCIE_RX4-	B55 B56	PCI Express channel 4, Receive Input differential pair	I PCIE		
PCIE_TX4+ PCIE_TX4-	A55 A56	PCI Express channel 4, Transmit Output differential pair	O PCIE		
PCIE_RX5+ PCIE_RX5-	B52 B53	PCI Express channel 5, Receive Input differential pair	I PCIE		Shared with SATA port 1 and configurable via the BIOS setup menu.
PCIE_TX5+ PCIE_TX5-	A52 A53	PCI Express channel 5, Transmit Output differential pair	O PCIE		
PCIE_RX6+ PCIE_RX6-	C19 C20	PCI Express channel 6, Receive Input differential pair	I PCIE		Shared with SATA port 0 and configurable via the BIOS setup menu.
PCIE_TX6+ PCIE_TX6-	D19 D20	PCI Express channel 6, Transmit Output differential pair	O PCIE		
PCIE_RX7+ PCIE_RX7-	C22 C23	PCI Express channel 7, Receive Input differential pair	I PCIE		Shared with USB 3.2 Gen 1x2, port 3 and configurable via the BIOS setup menu.
PCIE_TX7+ PCIE_TX7-	D22 D23	PCI Express channel 7, Transmit Output differential pair	O PCIE		
PCIE_CLK_REF+ PCIE_CLK_REF-	A88 A89	PCI Express Reference Clock output for all PCI Express and PCI Express Graphics Lanes	O PCIE		A PCI Express Gen2/3 compliant clock buffer chip must be used on the carrier board if the design involves more than one PCI Express device.

 **Note**

*The default BIOS setting for the shared ports is PCIe.*

Table 16 PCI Express Signal Descriptions (x16 Graphics)

Signal	Pin #	Description	I/O	PU/PD	Comment
PEG_RX0+	C52	PCI Express Graphics differential pairs 0 <i>Note: Can also be used as PCI Express differential pairs 16</i>		I PCIE	PCI Express Gen 3
PEG_RX0-	C53			O PCIE	
PEG_TX0+	D52			O PCIE	
PEG_TX0-	D53				
PEG_RX1+	C55	PCI Express Graphics differential pairs 1 <i>Note: Can also be used as PCI Express differential pairs 17</i>		I PCIE	
PEG_RX1-	C56				
PEG_TX1+	D55			O PCIE	
PEG_TX1-	D56				
PEG_RX2+	C58	PCI Express Graphics differential pairs 2 <i>Note: Can also be used as PCI Express differential pairs 18</i>		I PCIE	
PEG_RX2-	C59				
PEG_TX2+	D58			O PCIE	
PEG_TX2-	D59				
PEG_RX3+	C61	PCI Express Graphics differential pairs 3 <i>Note: Can also be used as PCI Express differential pairs 19</i>		I PCIE	
PEG_RX3-	C62				
PEG_TX3+	D61			O PCIE	
PEG_TX3-	D62				
PEG_RX4+	C65	PCI Express Graphics differential pairs 4 <i>Note: Can also be used as PCI Express differential pairs 20</i>		I PCIE	Not connected
PEG_RX4-	C66				
PEG_TX4+	D65			O PCIE	
PEG_TX4-	D66				
PEG_RX5+	C68	PCI Express Graphics differential pairs 5 <i>Note: Can also be used as PCI Express differential pairs 21</i>		I PCIE	
PEG_RX5-	C69				
PEG_TX5+	D68			O PCIE	
PEG_TX5-	D69				
PEG_RX6+	C71	PCI Express Graphics differential pairs 6 <i>Note: Can also be used as PCI Express differential pairs 22</i>		I PCIE	
PEG_RX6-	C72				
PEG_TX6+	D71			O PCIE	
PEG_TX6-	D72				
PEG_RX7+	C74	PCI Express Graphics differential pairs 7 <i>Note: Can also be used as PCI Express differential pairs 23</i>		I PCIE	
PEG_RX7-	C75				
PEG_TX7+	D74			O PCIE	
PEG_TX7-	D75				
PEG_RX8+	C78	PCI Express Graphics differential pairs 8 <i>Note: Can also be used as PCI Express differential pairs 24</i>		I PCIE	
PEG_RX8-	C79				
PEG_TX8+	D78			O PCIE	
PEG_TX8-	D79				
PEG_RX9+	C81	PCI Express Graphics differential pairs 9 <i>Note: Can also be used as PCI Express differential pairs 25</i>		I PCIE	
PEG_RX9-	C82				
PEG_TX9+	D81			O PCIE	
PEG_TX9-	D82				

Signal	Pin #	Description	I/O	PU/PD	Comment
PEG_RX10+	C85	PCI Express Graphics differential pairs 10 <i>Note: Can also be used as PCI Express differential pairs 26</i>		I PCIE	Not connected
PEG_RX10-	C86			O PCIE	
PEG_TX10+	D85			I PCIE	
PEG_TX10-	D86			O PCIE	
PEG_RX11+	C88	PCI Express Graphics differential pairs 11 <i>Note: Can also be used as PCI Express differential pairs 27</i>		I PCIE	
PEG_RX11-	C89			O PCIE	
PEG_TX11+	D88			I PCIE	
PEG_TX11-	D89			O PCIE	
PEG_RX12+	C91	PCI Express Graphics differential pairs 12 <i>Note: Can also be used as PCI Express differential pairs 28</i>		I PCIE	
PEG_RX12-	C92			O PCIE	
PEG_TX12+	D91			I PCIE	
PEG_TX12-	D92			O PCIE	
PEG_RX13+	C94	PCI Express Graphics differential pairs 13 <i>Note: Can also be used as PCI Express differential pairs 29</i>		I PCIE	
PEG_RX13-	C95			O PCIE	
PEG_TX13+	D94			I PCIE	
PEG_TX13-	D95			O PCIE	
PEG_RX14+	C98	PCI Express Graphics differential pairs 14 <i>Note: Can also be used as PCI Express differential pairs 30</i>		I PCIE	
PEG_RX14-	C99			O PCIE	
PEG_TX14+	D98			I PCIE	
PEG_TX14-	D99			O PCIE	
PEG_RX15+	C101	PCI Express Graphics differential pairs 15 <i>Note: Can also be used as PCI Express differential pairs 31</i>		I PCIE	
PEG_RX15-	C102			O PCIE	
PEG_TX15+	D101			I	
PEG_TX15-	D102				
PEG_LANE_RV#	D54	PCI Express Graphics lane reversal input strap. Pull low on the carrier board to reverse lane order.	I		Not supported

 **Note**

The conga-TC570 supports only PEG ports 0-3.

Table 17 DDI Signal Description

Signal	Pin #	Description	I/O	PU/PD	Comment
DDI1_PAIR0+ DDI1_PAIR0-	D26 D27	Multiplexed with DP1_LANE0+ and TMDS1_DATA2+ Multiplexed with DP1_LANE0- and TMDS1_DATA2-	O PCIE		
DDI1_PAIR1+ DDI1_PAIR1-	D29 D30	Multiplexed with DP1_LANE1+ and TMDS1_DATA1+ Multiplexed with DP1_LANE1- and TMDS1_DATA1-	O PCIE		
DDI1_PAIR2+ DDI1_PAIR2-	D32 D33	Multiplexed with DP1_LANE2+ and TMDS1_DATA0+ Multiplexed with DP1_LANE2- and TMDS1_DATA0-	O PCIE		
DDI1_PAIR3+ DDI1_PAIR3-	D36 D37	Multiplexed with DP1_LANE3+ and TMDS1_CLK+ Multiplexed with DP1_LANE3- and TMDS1_CLK-	O PCIE		
DDI1_PAIR4+ DDI1_PAIR4-	C25 C26	Digital Display Interface 1, differential pair 4			Not connected
DDI1_PAIR5+ DDI1_PAIR5-	C29 C30	Digital Display Interface 1, differential pair 5			Not connected
DDI1_PAIR6+ DDI1_PAIR6-	C15 C16	Digital Display Interface 1, differential pair 6			Not connected
DDI1_HPD	C24	Multiplexed with DP1_HPD and HDMI1_HPD	I 3.3 V	PD 1 MΩ	
DDI1_CTRLCLK_AUX+	D15	Multiplexed with DP1_AUX+ and HDMI1_CTRLCLK. DP AUX+ function if DDI1_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLCLK if DDI1_DDC_AUX_SEL is pulled high.	I/O PCIE I/O OD 3.3 V	PD 100 kΩ	
DDI1_CTRLDATA_AUX- <sup>1</sup>	D16	Multiplexed with DP1_AUX- and HDMI1_CTRLDATA. DP AUX- function if DDI1_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLDATA if DDI1_DDC_AUX_SEL is pulled high.	I/O PCIE I/O OD 3.3 V	PU 100 kΩ 3.3V	Bootstrap signal (see note below). DDI enable strap already populated.
DDI1_DDC_AUX_SEL	D34	Selects the function of DDI1_CTRLCLK_AUX+ and DDI1_CTRLDATA_AUX-. This pin shall have a 1M pull-down to logic ground on the module. If this input is floating, the AUX pair is used for the DP AUX+/- signals. If pulled-high, the AUX pair contains the CTRLCLK and CTRLDATA signals.	I 3.3 V	PD 1 MΩ	
DDI2_PAIR0+ DDI2_PAIR0-	D39 D40	Multiplexed with DP2_LANE0+ and TMDS2_DATA2+ Multiplexed with DP2_LANE0- and TMDS2_DATA2-	O PCIE		
DDI2_PAIR1+ DDI2_PAIR1-	D42 D43	Multiplexed with DP2_LANE1+ and TMDS2_DATA1+ Multiplexed with DP2_LANE1- and TMDS2_DATA1-	O PCIE		
DDI2_PAIR2+ DDI2_PAIR2-	D46 D47	Multiplexed with DP2_LANE2+ and TMDS2_DATA0+ Multiplexed with DP2_LANE2- and TMDS2_DATA0-	O PCIE		
DDI2_PAIR3+ DDI2_PAIR3-	D49 D50	Multiplexed with DP2_LANE3+ and TMDS2_CLK+ Multiplexed with DP2_LANE3- and TMDS2_CLK-	O PCIE		
DDI2_HPD	D44	Multiplexed with DP2_HPD and HDMI2_HPD	I 3.3 V	PD 1 MΩ	
DDI2_CTRLCLK_AUX+	C32	Multiplexed with DP2_AUX+ and HDMI2_CTRLCLK. DP AUX+ function if DDI2_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLCLK if DDI2_DDC_AUX_SEL is pulled high	I/O PCIE I/O OD 3.3 V	PD 100 kΩ	
DDI2_CTRLDATA_AUX- <sup>1</sup>	C33	Multiplexed with DP2_AUX- and HDMI2_CTRLDATA. DP AUX- function if DDI2_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLDATA if DDI2_DDC_AUX_SEL is pulled high.	I/O PCIE I/O OD 3.3 V	PU 100 kΩ 3.3 V	Bootstrap signal (see note below). DDI enable strap already populated.

Signal	Pin #	Description	I/O	PU/PD	Comment
DDI2_DDC_AUX_SEL	C34	Selects the function of DDI2_CTRLCLK_AUX+ and DDI2_CTRLDATA_AUX-. This pin shall have a 1M pull-down to logic ground on the module. If this input is floating, the AUX pair is used for the DP AUX+/- signals. If pulled-high, the AUX pair contains the CTRLCLK and CTRLDATA signals.	I 3.3V	PD 1 MΩ	
DDI3_PAIR0+ DDI3_PAIR0-	C39 C40	Multiplexed with DP3_LANE0+ and TMDS3_DATA2+ Multiplexed with DP3_LANE0- and TMDS3_DATA2-	O PCIE		
DDI3_PAIR1+ DDI3_PAIR1-	C42 C43	Multiplexed with DP3_LANE1+ and TMDS3_DATA1+ Multiplexed with DP3_LANE1- and TMDS3_DATA1-	O PCIE		
DDI3_PAIR2+ DDI3_PAIR2-	C46 C47	Multiplexed with DP3_LANE2+ and TMDS3_DATA0+ Multiplexed with DP3_LANE2- and TMDS3_DATA0-	O PCIE		
DDI3_PAIR3+ DDI3_PAIR3-	C49 C50	Multiplexed with DP3_LANE3+ and TMDS3_CLK+ Multiplexed with DP3_LANE3- and TMDS3_CLK-	O PCIE		
DDI3_HPD	C44	Multiplexed with DP3_HPD and HDMI3_HPD	I 3.3 V	PD 1 MΩ	
DDI3_CTRLCLK_AUX+	C36	Multiplexed with DP3_AUX+ and HDMI3_CTRLCLK. DP AUX+ function if DDI3_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLCLK if DDI3_DDC_AUX_SEL is pulled high.	I/O PCIE I/O OD 3.3 V	PD 100 kΩ	
DDI3_CTRLDATA_AUX- <sup>1</sup>	C37	Multiplexed with DP3_AUX- and HDMI3_CTRLDATA. DP AUX- function if DDI3_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLDATA if DDI3_DDC_AUX_SEL is pulled high.	I/O PCIE I/O OD 3.3 V	PU 100 kΩ 3.3 V	Bootstrap signal (see note below). DDI enable strap already populated.
DDI3_DDC_AUX_SEL	C38	Selects the function of DDI3_CTRLCLK_AUX+ and DDI3_CTRLDATA_AUX-. This pin shall have a 1M pull-down to logic ground on the module. If this input is floating, the AUX pair is used for the DP AUX+/- signals. If pulled-high, the AUX pair contains the CTRLCLK and CTRLDATA signals.	I 3.3 V	PD 1 MΩ	



<sup>1</sup>. These signals have special functionality during the reset process. They may bootstrap some basic important functions of the module. For more information refer to section 8.2 "Bootstrap Signals".

Table 18 TMDS Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
TMDS1_CLK + TMDS1_CLK -	D36 D37	TMDS Clock output differential pair Multiplexed with DDI1_PAIR3+ and DDI1_PAIR3-	O PCIE		
TMDS1_DATA0+ TMDS1_DATA0-	D32 D33	TMDS differential pair Multiplexed with DDI1_PAIR2+ and DDI1_PAIR2-	O PCIE		
TMDS1_DATA1+ TMDS1_DATA1-	D29 D30	TMDS differential pair Multiplexed with DDI1_PAIR1+ and DDI1_PAIR1-	O PCIE		
TMDS1_DATA2+ TMDS1_DATA2-	D26 D27	TMDS differential pair Multiplexed with DDI1_PAIR0+ and DDI1_PAIR0-	O PCIE		

Signal	Pin #	Description	I/O	PU/PD	Comment
HDMI1_HPD	C24	TMDS Hot-plug detect Multiplexed with DDI1_HPD	I PCIE	PD 1 M $\Omega$	
HDMI1_CTRLCLK	D15	TMDS I <sup>2</sup> C Control Clock Multiplexed with DDI1_CTRLCLK_AUX+	I/O OD 3.3 V	PD 100 k $\Omega$	
HDMI1_CTRLDATA <sup>1</sup>	D16	TMDS I <sup>2</sup> C Control Data Multiplexed with DDI1_CTRLDATA_AUX-	I/O OD 3.3 V	PU 100 k $\Omega$ 3.3 V	Bootstrap signal (see note below). Enable strap is already populated
TMDS2_CLK + TMDS2_CLK -	D49 D50	TMDS Clock output differential pair Multiplexed with DDI2_PAIR3+ and DDI2_PAIR3-	O PCIE		
TMDS2_DATA0+ TMDS2_DATA0-	D46 D47	TMDS differential pair Multiplexed with DDI2_PAIR2+ and DDI2_PAIR2-	O PCIE		
TMDS2_DATA1+ TMDS2_DATA1-	D42 D43	TMDS differential pair Multiplexed with DDI2_PAIR1+ and DDI2_PAIR1-	O PCIE		
TMDS2_DATA2+ TMDS2_DATA2-	D39 D40	TMDS differential pair Multiplexed with DDI2_PAIR0+ and DDI2_PAIR0-	O PCIE		
HDMI2_HPD	D44	TMDS Hot-plug detect. Multiplexed with DDI2_HPD	I PCIE	PD 1 M $\Omega$	
HDMI2_CTRLCLK	C32	TMDS I <sup>2</sup> C Control Clock Multiplexed with DDI2_CTRLCLK_AUX+	I/O OD 3.3 V	PD 100 k $\Omega$	
HDMI2_CTRLDATA <sup>1</sup>	C33	TMDS I <sup>2</sup> C Control Data Multiplexed with DDI2_CTRLDATA_AUX-	I/O OD 3.3 V	PU 100 k $\Omega$ 3.3 V	Bootstrap signal (see note below). Enable strap is already populated.
TMDS3_CLK + TMDS3_CLK -	C49 C50	TMDS Clock output differential pair Multiplexed with DDI3_PAIR3+ and DDI3_PAIR3-	O PCIE		
TMDS3_DATA0+ TMDS3_DATA0-	C46 C47	TMDS differential pair Multiplexed with DDI3_PAIR2+ and DDI3_PAIR2-	O PCIE		
TMDS3_DATA1+ TMDS3_DATA1-	C42 C43	TMDS differential pair Multiplexed with DDI3_PAIR1+ and DDI3_PAIR1-	O PCIE		
TMDS3_DATA2+ TMDS3_DATA2-	C39 C40	TMDS differential pair Multiplexed with DDI3_PAIR0+ and DDI3_PAIR0-	O PCIE		
HDMI3_HPD	C44	TMDS Hot-plug detect Multiplexed with DDI3_HPD	I PCIE	PD 1 M $\Omega$	
HDMI3_CTRLCLK	C36	TMDS I <sup>2</sup> C Control Clock Multiplexed with DDI3_CTRLCLK_AUX+	I/O OD 3.3 V	PD 100 k $\Omega$	
HDMI3_CTRLDATA <sup>1</sup>	C37	TMDS I <sup>2</sup> C Control Data Multiplexed with DDI3_CTRLDATA_AUX-	I/O OD 3.3 V	PU 100 k $\Omega$ 3.3 V	Bootstrap signal (see note below). Enable strap is already populated.

 **Note**

<sup>1</sup>. These signals have special functionality during the reset process. They may bootstrap some basic important functions of the module. For more information refer to section 8.2 "Bootstrap Signals".

Table 19 DisplayPort (DP) Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
DP1_LANE3+ DP1_LANE3-	D36 D37	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI1_PAIR3+ and DDI1_PAIR3-	O PCIE		
DP1_LANE2+ DP1_LANE2-	D32 D33	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI1_PAIR2+ and DDI1_PAIR2-	O PCIE		
DP1_LANE1+ DP1_LANE1-	D29 D30	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI1_PAIR1+ and DDI1_PAIR1-	O PCIE		
DP1_LANE0+ DP1_LANE0-	D26 D27	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI1_PAIR0+ and DDI1_PAIR0-	O PCIE		
DP1_HPD	C24	Detection of Hot Plug / Unplug and notification of the link layer. Multiplexed with DDI1_HPD	I 3.3 V	PD 1 M $\Omega$	
DP1_AUX+	D15	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access.	I/O PCIE	PD 100 k $\Omega$	
DP1_AUX- <sup>1</sup>	D16	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access.	I/O PCIE	PU 100 k $\Omega$ 3.3 V	Bootstrap signal (see note below). DP enable strap is already populated.
DP2_LANE3+ DP2_LANE3-	D49 D50	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI2_PAIR3+ and DDI2_PAIR3-	O PCIE		
DP2_LANE2+ DP2_LANE2-	D46 D47	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI2_PAIR2+ and DDI2_PAIR2-	O PCIE		
DP2_LANE1+ DP2_LANE1-	D42 D43	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI2_PAIR1+ and DDI2_PAIR1-	O PCIE		
DP2_LANE0+ DP2_LANE0-	D39 D40	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI2_PAIR0+ and DDI1_PAIR0-	O PCIE		
DP2_HPD	D44	Detection of Hot Plug / Unplug and notification of the link layer. Multiplexed with DDI2_HPD	I 3.3 V	PD 1 M $\Omega$	
DP2_AUX+	C32	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access.	I/O PCIE	PD 100 k $\Omega$	
DP2_AUX- <sup>1</sup>	C33	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access.	I/O PCIE	PU 100 k $\Omega$ 3.3 V	Bootstrap signal (see note below). DP enable strap is already populated.
DP3_LANE3+ DP3_LANE3-	C49 C50	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI3_PAIR3+ and DDI3_PAIR3-	O PCIE		

Signal	Pin #	Description	I/O	PU/PD	Comment
DP3_LANE2+ DP3_LANE2-	C46 C47	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI3_PAIR2+ and DDI3_PAIR2-	O PCIE		
DP3_LANE1+ DP3_LANE1-	C42 C43	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI3_PAIR1+ and DDI3_PAIR1-	O PCIE		
DP3_LANE0+ DP3_LANE0-	C39 C40	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI3_PAIR0+ and DDI3_PAIR0-	O PCIE		
DP3_HPD	C44	Detection of Hot Plug / Unplug and notification of the link layer. Multiplexed with DDI3_HPD	I 3.3 V	PD 1 MΩ	
DP3_AUX+	C36	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access.	I/O PCIE	PD 100 kΩ	
DP3_AUX- <sup>1</sup>	C37	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access.	I/O PCIE	PU 100 kΩ 3.3 V	Bootstrap signal (see note below). DP enable strap is already populated.



### Note

- <sup>1</sup> These signals have special functionality during the reset process. They may bootstrap some basic important functions of the module. For more information refer to section 8.2 "Bootstrap Signals".

Table 20 Embedded DisplayPort Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
eDP_TX3+ eDP_TX3- eDP_TX2+ eDP_TX2- eDP_TX1+ eDP_TX1- eDP_TX0+ eDP_TX0-	A81 A82 A71 A72 A73 A74 A75 A76	eDP differential pairs	AC coupled off module.		
eDP_VDD_EN	A77	eDP power enable	O 3.3 V		
eDP_BKLT_EN	B79	eDP backlight enable	O 3.3 V		
eDP_BKLT_CTRL	B83	eDP backlight brightness control	O 3.3 V		
eDP_AUX+	A83	eDP AUX+	AC coupled off module		
eDP_AUX-	A84	eDP AUX-	AC coupled off module		
eDP_HPD	A87	Detection of hot plug / unplug and notification of the link layer	I 3.3 V	PD 1 MΩ	

Table 21 CRT Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
VGA_RED	B89	Red for monitor; analog DAC output designed to drive a 37.5-Ohm equivalent load	O Analog	PD 150R	Commercial variants only
VGA_GRN	B91	Green for monitor; analog DAC output designed to drive a 37.5-Ohm equivalent load	O Analog	PD 150R	
VGA_BLU	B92	Blue for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load	O Analog	PD 150R	
VGA_HSYNC	B93	Horizontal sync output to VGA monitor	O 3.3 V		
VGA_VSYNC	B94	Vertical sync output to VGA monitor	O 3.3 V		
VGA_I2C_CK	B95	DDC clock line (I <sup>2</sup> C port dedicated to identify VGA monitor capabilities)	I/O OD 5 V	PU 2k2 3.3 V	
VGA_I2C_DAT	B96	DDC data line	I/O OD 5 V	PU 2k2 3.3 V	



**Note**

To support the VGA interface on industrial variants, you need a customized conga-TC570 variant (assembly option).

Table 22 LVDS Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
LVDS_A0+	A71	LVDS Channel A differential pairs	O LVDS		
LVDS_A0-	A72				
LVDS_A1+	A73				
LVDS_A1-	A74				
LVDS_A2+	A75				
LVDS_A2-	A76				
LVDS_A3+	A78				
LVDS_A3-	A79				
LVDS_A_CK+	A81	LVDS Channel A differential clock	O LVDS		
LVDS_A_CK-	A82				
LVDS_B0+	B71	LVDS Channel B differential pairs	O LVDS		
LVDS_B0-	B72				
LVDS_B1+	B73				
LVDS_B1-	B74				
LVDS_B2+	B75				
LVDS_B2-	B76				
LVDS_B3+	B77				
LVDS_B3-	B78				
LVDS_B_CK+	B81	LVDS Channel B differential clock	O LVDS		
LVDS_B_CK-	B82				
LVDS_VDD_EN	A77	LVDS panel power enable	O 3.3 V		
LVDS_BKLT_EN	B79	LVDS panel backlight enable	O 3.3 V		
LVDS_BKLT_CTRL	B83	LVDS panel backlight brightness control	O 3.3 V		
LVDS_I2C_CK	A83	DDC lines used for flat panel detection and control	I/O 3.3 V	PU 2k2 3.3 V	PU for LVDS support (default)
LVDS_I2C_DAT	A84	DDC lines used for flat panel detection and control	I/O 3.3 V	PU 2k2 3.3 V	PU for LVDS support (default)

**Table 23 Serial ATA Signal Descriptions**

Signal	Pin #	Description	I/O	PU/PD	Comment
SATA0_RX+	A19	Serial ATA channel 0, receive input differential pair	I SATA		Shared with PCIe lane 6
SATA0_RX-	A20				
SATA0_TX+	A16	Serial ATA channel 0, transmit output differential pair	O SATA		
SATA0_TX-	A17				
SATA1_RX+	B19	Serial ATA channel 1, receive input differential pair	I SATA		Shared with PCIe lane 5
SATA1_RX-	B20				
SATA1_TX+	B16	Serial ATA channel 1, transmit output differential pair	O SATA		
SATA1_TX-	B17				
SATA2_RX+	A25	Serial ATA channel 2, receive input differential pair	I SATA		Not connected
SATA2_RX-	A26				
SATA2_TX+	A22	Serial ATA channel 2, transmit output differential pair	O SATA		
SATA2_TX-	A23				
SATA3_RX+	B25	Serial ATA channel 3, receive input differential pair	I SATA		Not connected
SATA3_RX-	B26				
SATA3_TX+	B22	Serial ATA channel 3, transmit output differential pair	O SATA		
SATA3_TX-	B23				
(S)ATA_ACT#	A28	Serial ATA activity indicator, active low	I/O 3.3 V		

**Table 24 USB 2.0 Signal Descriptions**

Signal	Pin #	Description	I/O	PU/PD	Comment
USB0+	B46	USB Port 0, data + or D+	I/O		
USB0-	B45	USB Port 0, data - or D-	I/O		
USB1+	A46	USB Port 1, data + or D+	I/O		
USB1-	A45	USB Port 1, data - or D-	I/O		
USB2+	A43	USB Port 2, data + or D+	I/O		
USB2-	A42	USB Port 2, data - or D-	I/O		
USB3+	B43	USB Port 3, data + or D+	I/O		
USB3-	B42	USB Port 3, data - or D-	I/O		
USB4+	A40	USB Port 4, data + or D+	I/O		
USB4-	A39	USB Port 4, data - or D-	I/O		
USB5+	B40	USB Port 5, data + or D+	I/O		
USB5-	B39	USB Port 5, data - or D-	I/O		
USB6+	A37	USB Port 6, data + or D+	I/O		
USB6-	A36	USB Port 6, data - or D-	I/O		
USB7+	B37	USB Port 7, data + or D+	I/O		
USB7-	B36	USB Port 7, data - or D-	I/O		

Signal	Pin #	Description	I/O	PU/PD	Comment
USB_0_1_OC# <sup>1</sup>	B44	USB over-current sense, USB ports 0 and 1. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3 VSB	PU 10 kΩ 3.3 VSB	Do not pull this line high on the carrier board
USB_2_3_OC# <sup>1</sup>	A44	USB over-current sense, USB ports 2 and 3. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low. .	I 3.3 VSB	PU 10 kΩ 3.3 VSB	Do not pull this line high on the carrier board
USB_4_5_OC# <sup>1</sup>	B38	USB over-current sense, USB ports 4 and 5. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3 VSB	PU 10 kΩ 3.3 VSB	Do not pull this line high on the carrier board
USB_6_7_OC# <sup>1</sup>	A38	USB over-current sense, USB ports 6 and 7. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3 VSB	PU 10 kΩ 3.3 VSB	Do not pull this line high on the carrier board
USB0_HOST_PRSENT	B48	Module USB client may detect the presence of a USB host on USB0. A high values indicates that a host is present.	I 3.3 VSB	PD 1 MΩ	Not Supported



### Note

- <sup>1</sup> These signals have special functionality during the reset process. They may bootstrap some basic important functions of the module. For more information refer to section 8.2 "Bootstrap Signals".

Table 25 USB 3.0 Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
USB_SSRX0+	C4	Additional receive signal differential pairs for the Superspeed USB data path	I		
USB_SSRX0-	C3		I		
USB_SSTX0+	D4	Additional transmit signal differential pairs for the Superspeed USB data path	O		
USB_SSTX0-	D3		O		
USB_SSRX1+	C7	Additional receive signal differential pairs for the Superspeed USB data path	I		
USB_SSRX1-	C6		I		
USB_SSTX1+	D7	Additional transmit signal differential pairs for the Superspeed USB data path	O		
USB_SSTX1-	D6		O		
USB_SSRX2+	C10	Additional receive signal differential pairs for the Superspeed USB data path	I		
USB_SSRX2-	C9		I		
USB_SSTX2+	D10	Additional transmit signal differential pairs for the Superspeed USB data path	O		
USB_SSTX2-	D9		O		
USB_SSRX3+	C13	Additional receive signal differential pairs for the Superspeed USB data path	I		Shared with PCIe lane 7 and configurable via the BIOS setup menu
USB_SSRX3-	C12		I		
USB_SSTX3+	D13	Additional transmit signal differential pairs for the Superspeed USB data path	O		
USB_SSTX3-	D12		O		

Table 26 Gigabit Ethernet Signal Descriptions

Gigabit Ethernet	Pin #	Description	I/O	PU/PD	Comment				
GBE0_MDI0+	A13	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0, 1, 2, 3. The MDI can operate in 1000, 100, and 10 Mbps modes. Some pairs are unused in some modes according to the following:	I/O Analog						
GBE0_MDI0-	A12								
GBE0_MDI1+	A10								
GBE0_MDI1-	A9						1000BASE-T	100BASE-TX	10BASE-T
GBE0_MDI2+	A7					MDI[0]+/-	B1_DA+/-	TX+/-	TX+/-
GBE0_MDI2-	A6					MDI[1]+/-	B1_DB+/-	RX+/-	RX+/-
GBE0_MDI3+	A3					MDI[2]+/-	B1_DC+/-		
GBE0_MDI3-	A2	MDI[3]+/-	B1_DD+/-						
GBE0_ACT#	B2	Gigabit Ethernet Controller 0 activity indicator, active low	OD 3.3 V						
GBE0_LINK# <sup>1,2</sup>	A8	Gigabit Ethernet Controller 0 link indicator, active low	OD 3.3 V						
GBE0_LINK100# <sup>2</sup>	A4	Gigabit Ethernet Controller 0 100 Mbps link indicator, active low	OD 3.3 V						
GBE0_LINK1000# <sup>2</sup>	A5	Gigabit Ethernet Controller 0 1000 Mbps link indicator, active low	OD 3.3 V						
GBE0_CTREF	A14	Reference voltage for Carrier Board Ethernet channel 0 magnetics center tap. The reference voltage is determined by the requirements of the module PHY and may be as low as 0 V and as high as 3.3 V. The reference voltage output shall be current limited on the module. In the case in which the reference is shorted to ground, the current shall be limited to 250 mA or less.	REF		Not connected				
GBE0_SDP	A49	Gigabit Ethernet Controller 0 Software-Definable Pin. Can also be used for IEEE1588 support such as a 1 pps signal.	I/O		Signal is provided by the Intel i225 controller				

 **Note**

- <sup>1</sup> The GBE0\_LINK# output is not active during a 10 Mb connection. It is only active during a 100 Mb or 1 Gb connection. This is a limitation of Ethernet Phy since it only has 3 LED outputs—ACT#, LINK100# and LINK1000#.
- <sup>2</sup> The GBE0\_LINK# signal is a logic AND of the GBE0\_LINK100# and GBE0\_LINK1000# signals on the conga-TC570 module.

Table 27 High Definition Audio Link Signals Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
HDA_RST# <sup>2</sup>	A30	Reset output to codec; active low	O 3.3 V		
HDA_SYNC <sup>2</sup>	A29	Sample-synchronization signal to the codec(s)	O 3.3 V		
HDA_BITCLK <sup>2</sup>	A32	Serial data clock generated by the external codec(s)	O 3.3 V		
HDA_SDOUT <sup>1,2</sup>	A33	Serial TDM data output to the codec	O 3.3 V		Bootstrap signal (see note below)
HDA_SDIN[1:0] <sup>1</sup>	B29-B30	Serial TDM data inputs from up to three codecs	I 3.3 V		Bootstrap signal (see note below) HDA_SDIN2 (pin B28) is not connected



**Note**

- <sup>1</sup> This signal has special functionality during the reset process. It may bootstrap some basic important functions of the module. For more information refer to section 8.2 "Bootstrap Signals".
- <sup>2</sup> AC'97 codecs are not supported.

Table 28 LPC Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
LPC_AD[0:3]	B4-B7	LPC Mode: LPC multiplexed address, command and data bus	I/O 3.3 V	PU 20 K $\Omega$ 3.3 V	
LPC_FRAME#	B3	LPC Mode: LPC Frame indicates the start of a LPC cycle	O 3.3 V		
LPC_CLK	B10	LPC Mode: LPC clock output, 33MHz	O 3.3 V		
LPC_DRQ[0:1]#	B8	LPC Mode: LPC serial DMA request	I 3.3 V	PU 10 K $\Omega$ 3.3 V	
LPC_SERIRQ	A50	LPC Mode: LPC serial interrupt	I/O 3.3 V	PU 10 K $\Omega$ 3.3 V	
SUS_STAT#	B18	LPC Mode: Indicates imminent suspend operation. It is used to notify LPC devices that a low power state will be entered soon. LPC devices may need to preserve memory or isolate outputs during the low power state.	O 3.3 V		
ESPI_EN# <sup>1</sup>	B47	This signal is used by the carrier to indicate the operating mode of the LPC/eSPI bus. If left unconnected on the carrier, LPC mode (default) is selected. If pulled to GND on the carrier, eSPI mode is selected. This signal is pulled to a logic high on the module through a resistor. The carrier should only float this line or pull it low.	I		Not connected



- <sup>1</sup> The conga-TC570 does not support ESPI mode.

Table 29 SPI BIOS Flash Interface Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SPI_CS#	B97	Chip select for Carrier Board SPI BIOS Flash	O 3.3 VSB		Carrier shall pull to SPI_POWER when external SPI is provided but not used
SPI_MISO <sup>1</sup>	A92	Data in to module from carrier board SPI BIOS flash	I 3.3 VSB		
SPI_MOSI <sup>1</sup>	A95	Data out from module to carrier board SPI BIOS flash	O 3.3 VSB	PU 4K75 3.3 VSB	SPI_MOSI is a bootstrap signal (see note below)
SPI_CLK	A94	Clock from module to carrier board SPI BIOS flash	O 3.3 VSB		
SPI_POWER	A91	Power source for carrier board SPI BIOS flash. SPI_POWER shall be used to power SPI BIOS flash on the carrier only.	3.3 VSB		
BIOS_DIS0#	A34	Selection strap to determine the BIOS boot device	I 3.3 VSB	PU 10 K $\Omega$ 3.3 VSB	Carrier shall be left as no-connect
BIOS_DIS1#	B88	Selection strap to determine the BIOS boot device. Refer to table 4.13 of the COM Express Module Base Specification 3.0 for strapping options of BIOS disable signals.	I 3.3 VSB	PU 10 K $\Omega$ 3.3 VSB	Carrier shall be left as no-connect



**Note**

<sup>1</sup> These signals have special functionality during the reset process. They may bootstrap some basic important functions of the module. For more information refer to section 8.2 “Bootstrap Signals”.

Table 30 Miscellaneous Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
I2C_CK	B33	General purpose I <sup>2</sup> C port clock output/input	I/O 3.3 V	PU 2K2 3.3 VSB	
I2C_DAT	B34	General purpose I <sup>2</sup> C port data I/O line	I/O 3.3 V	PU 2K2 3.3 VSB	
SPKR <sup>1</sup>	B32	Output for audio enunciator, the “speaker” in PC-AT systems	O 3.3 V		Bootstrap signal (see note below)
WDT	B27	Output indicating that a watchdog time-out event has occurred	O 3.3 V	PD 100 K $\Omega$	
FAN_PWMOUT <sup>2</sup>	B101	Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan’s RPM.	O OD 3.3 V		
FAN_TACHIN <sup>2</sup>	B102	Fan tachometer input	I OD	PU 47K5 3.3 V	Requires a fan with a two pulse output
TPM_PP	A96	Physical Presence pin of Trusted Platform Module (TPM). Active high. TPM chip has an internal pull-down. This signal is used to indicate Physical Presence to the TPM.	I 3.3 V	PD 1 K $\Omega$	



**Note**

<sup>1</sup> This signal has special functionality during the reset process. It may bootstrap some basic important functions of the module. For more information refer to section 8.2 “Bootstrap Signals”.

<sup>2</sup> Pins are protected on the module by a series schottky diode. Therefore, pull-down resistor is required on the carrier board for proper logic level.

**Table 31 General Purpose I/O Signal Descriptions**

Signal	Pin #	Description	I/O	PU/PD	Comment
GPO0	A93	General purpose output pins Shared with SD_CLK. Output from COM Express, input to SD.	O 3.3 V		
GPO1	B54	General purpose output pins Shared with SD_CMD. Output from COM Express, input to SD.	O 3.3 V		
GPO2	B57	General purpose output pins Shared with SD_WP. Output from COM Express, input to SD.	O 3.3 V		
GPO3	B63	General purpose output pins Shared with SD_CD. Output from COM Express, input to SD.	O 3.3 V		
GPI0	A54	General purpose input pins Pulled high internally on the module. Shared with SD_DATA0. Bidirectional signal.	I 3.3 V	PU 10K $\Omega$ 3.3 V	
GPI1	A63	General purpose input pins Pulled high internally on the module. Shared with SD_DATA1. Bidirectional signal.	I 3.3 V	PU 10K $\Omega$ 3.3 V	
GPI2	A67	General purpose input pins Pulled high internally on the module. Shared with SD_DATA2. Bidirectional signal.	I 3.3 V	PU 10K $\Omega$ 3.3 V	
GPI3	A85	General purpose input pins Pulled high internally on the module. Shared with SD_DATA3. Bidirectional signal.	I 3.3 V	PU 10K $\Omega$ 3.3 V	



*The conga-TC570 provides GPIO signals on the COM Express connector by default.*

**Table 32 Power and System Management Signal Descriptions**

Signal	Pin #	Description	I/O	PU/PD	Comment
PWRBTN#	B12	Power button to bring system out of S5 (soft off), active on falling edge Note: For proper detection, assert a pulse width of at least 16 ms	I 3.3 VSB	PU 100 k $\Omega$ 3.3 VSB	
SYS_RESET#	B49	Reset button input. Active low input. Edge triggered. System will not be held in hardware reset while this input is kept low. Note: For proper detection, assert a pulse width of at least 16 ms.	I 3.3 VSB	PU 10 k $\Omega$ 3.3 VSB	
CB_RESET#	B50	Reset output from module to Carrier Board. Active low. Issued by module chipset and may result from a low SYS_RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the module software.	O 3.3 V	PD 100 k $\Omega$	
PWR_OK	B24	Power OK from main power supply. A high value indicates that the power is good	I 3.3 V		Set by resistor divider to accept 3.3V

Signal	Pin #	Description	I/O	PU/PD	Comment
SUS_STAT#	B18	Indicates imminent suspend operation; used to notify LPC devices	O 3.3 VSB		
SUS_S3#	A15	Indicates system is in Suspend to RAM state. Active-low output. An inverted copy of SUS_S3# on the carrier board (also known as "PS_ON") may be used to enable the non-standby power on a typical ATX power supply.	O 3.3 VSB		
SUS_S4#	A18	Indicates system is in Suspend to Disk state. Active low output	O 3.3 VSB		Not supported
SUS_S5#	A24	Indicates system is in Soft Off state	O 3.3 VSB		
WAKE0#	B66	PCI Express wake up signal	I 3.3 VSB	PU 1 k $\Omega$ 3.3 VSB	
WAKE1#	B67	General purpose wake up signal. May be used to implement wake-up on PS/2 keyboard or mouse activity.	I 3.3 VSB	PU 10 k $\Omega$ 3.3 VSB	
BATLOW#	A27	Battery low input. This signal may be driven low by external circuitry to signal that the system battery is low, or may be used to signal some other external power-management event.	I 3.3 VSB	PU 10 k $\Omega$ 3.3 VSB	
LID#	A103	Lid button. Used by the ACPI operating system for a LID switch. Note: For proper detection, assert a pulse width of at least 16 ms.	I OD 3.3 V	PU 10 k $\Omega$ 3.3 VSB	
SLEEP#	B103	Sleep button. Used by the ACPI operating system to bring the system to sleep state or to wake it up again. Note: For proper detection, assert a pulse width of at least 16 ms.	I OD 3.3 V	PU 100 k $\Omega$ 3.3 VSB	

Table 33 Rapid Shutdown Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
RAPID_SHUTDOWN	C67	Trigger for Rapid Shutdown. Must be driven to 5V through a $\leq 50$ ohm source impedance for $\geq 20$ $\mu$ s.	I 3.3 V		Not connected



*The conga-TC570 does not support Rapid Shutdown.*

Table 34 Thermal Protection Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
THRM#	B35	Input from off-module temp sensor indicating an over-temp situation	I 3.3 V	PU 10 k $\Omega$ 3.3 V	
THRMTRIP#	A35	Active low output indicating that the CPU has entered thermal shutdown	O 3.3 V	PU 10 k $\Omega$ 3.3 V	

Table 35 SMBus Signal Description

Signal	Pin #	Description	I/O	PU/PD	Comment
SMB_CK	B13	System Management Bus bidirectional clock line.	I/O 3.3 VSB	PU 100 kΩ 3.3 VSB	
SMB_DAT#	B14	System Management Bus bidirectional data line.	I/O OD 3.3 VSB	PU 100 kΩ 3.3 VSB	
SMB_ALERT#	B15	System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system.	I 3.3 VSB	PU 100 kΩ 3.3 VSB	

Table 36 General Purpose Serial Interface Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SER0_TX <sup>1</sup>	A98	General purpose serial port transmitter	O 3.3 V		This pin is protected on the module by a series schottky diode. Pulldown resistor is therefore required on the carrier for proper logic level.
SER1_TX <sup>1</sup>	A101	General purpose serial port transmitter	O 3.3 V		
SER0_RX <sup>1</sup>	A99	General purpose serial port receiver	I 3.3 V	PU 47K5 3.3 V	
SER1_RX <sup>1</sup>	A102	General purpose serial port receiver	I 3.3 V	PU 47K5 3.3 V	



**Note**

<sup>1</sup>. Pins are protected on the module by a series schottky diode. Therefore, pull-down resistor is required on the carrier board for proper logic level.

Table 37 Module Type Definition Signal Description

Signal	Pin #	Description	I/O	Comment																												
TYPE0# TYPE1# TYPE2#	C54 C57 D57	<p>The TYPE pins indicate to the carrier board the pinout type that is implemented on the module.</p> <p>The pins are tied on the module to either ground (GND) or are no-connects (NC). For pinout Type 1, these pins are don't care (X).</p> <table border="1"> <thead> <tr> <th>TYPE2#</th> <th>TYPE1#</th> <th>TYPE0#</th> <th></th> </tr> </thead> <tbody> <tr> <td>X</td> <td>X</td> <td>X</td> <td>Pinout Type 1</td> </tr> <tr> <td>NC</td> <td>NC</td> <td>NC</td> <td>Pinout Type 2</td> </tr> <tr> <td>NC</td> <td>NC</td> <td>GND</td> <td>Pinout Type 3 (no IDE)</td> </tr> <tr> <td>NC</td> <td>GND</td> <td>NC</td> <td>Pinout Type 4 (no PCI)</td> </tr> <tr> <td>NC</td> <td>GND</td> <td>GND</td> <td>Pinout Type 5 (no IDE, no PCI)</td> </tr> <tr> <td>GND</td> <td>NC</td> <td>NC</td> <td>Pinout Type 6 (no IDE, no PCI)</td> </tr> </tbody> </table> <p>The carrier board should implement combinatorial logic that monitors the module 'TYPE' pins and keeps power off (e.g deactivates the ATX_ON signal for an ATX power supply) if an incompatible module pin-out type is detected.</p> <p>The carrier board logic may also implement a fault indicator such as an LED.</p>	TYPE2#	TYPE1#	TYPE0#		X	X	X	Pinout Type 1	NC	NC	NC	Pinout Type 2	NC	NC	GND	Pinout Type 3 (no IDE)	NC	GND	NC	Pinout Type 4 (no PCI)	NC	GND	GND	Pinout Type 5 (no IDE, no PCI)	GND	NC	NC	Pinout Type 6 (no IDE, no PCI)	PDS	<p>TYPE[0:2]# signals are available on all modules following the Type 2-6 Pinout standard.</p> <p>The conga-TC570 is based on the COM Express Type 6 pinout therefore the pins 0 and 1 are not connected and pin 2 is connected to GND.</p>
TYPE2#	TYPE1#	TYPE0#																														
X	X	X	Pinout Type 1																													
NC	NC	NC	Pinout Type 2																													
NC	NC	GND	Pinout Type 3 (no IDE)																													
NC	GND	NC	Pinout Type 4 (no PCI)																													
NC	GND	GND	Pinout Type 5 (no IDE, no PCI)																													
GND	NC	NC	Pinout Type 6 (no IDE, no PCI)																													
TYPE10#	A97	<p>Dual use pin.</p> <p>Indicates to the carrier board that a Type 10 module is installed.</p> <p>Indicates to the carrier that a Rev. 1.0/2.0 module is installed.</p> <table border="1"> <thead> <tr> <th>TYPE10#</th> <th></th> </tr> </thead> <tbody> <tr> <td>NC</td> <td>Pinout R2.0</td> </tr> <tr> <td>PD</td> <td>Pinout Type 10 pull down to ground with 4.7k resistor</td> </tr> <tr> <td>12V</td> <td>Pinout R1.0</td> </tr> </tbody> </table> <p>This pin is reclaimed from VCC_12V pool. In R1.0 modules this pin will connect to other VCC_12V pins.</p> <p>In R2.0 this pin is defined as a no-connect for Types 1-6. A carrier can detect a R1.0 module by the presence of 12 V on this pin. R2.0 module Types 1-6 will no-connect this pin. Type 10 modules shall pull this pin to ground through a 4.7 kΩ resistor.</p>	TYPE10#		NC	Pinout R2.0	PD	Pinout Type 10 pull down to ground with 4.7k resistor	12V	Pinout R1.0	PDS	Not connected to indicate "Pinout R2.0".																				
TYPE10#																																
NC	Pinout R2.0																															
PD	Pinout Type 10 pull down to ground with 4.7k resistor																															
12V	Pinout R1.0																															

Table 38 Power and GND Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
VCC_12V	A104-A109 B104-B109 C104-C109 D104-D109	Primary power input: +12V nominal. All available VCC_12V pins on the connector(s) shall be used.	P		
VCC_5V_SBY	B84-B87	Standby power input: +5.0V nominal. If VCC5_SBY is used, all available VCC_5V_SBY pins on the connector(s) shall be used. Only used for standby and suspend functions. May be left unconnected if these functions are not used in the system design.	P		
VCC_RTC	A47	Real-time clock circuit-power input. Nominally +3.0V.	P		
GND	A1, A11, A21, A31, A41, A51, A57, A60, A66, A70, A80, A90, A100, A110, B1, B11, B21, B31, B41, B51, B60, B70, B80, B90, B100, B110 C1, C2, C5, C8, C11, C14, C21, C31, C41, C51, C60, C70, C73, C76, C80, C84, C87, C90, C93, C96, C100, C103, C110, D1, D2, D5, D8, D11, D14, D21, D31, D41, D51, D60, D67, D70, D73, D76, D80, D84, D87, D90, D93, D96, D100, D103, D110	Ground: DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to Carrier Board GND plane.	P		

## 8.2 Bootstrap Signals

Table 39 Bootstrap Signal Descriptions

Signal	Pin #	Description of Bootstrap Signal	I/O	PU/PD	Comment
HDA_SDOUT	A33	High Definition Audio Serial Data Output	O 3.3 VSB		
SPKR	B32	Output for audio enunciator, the "speaker" in PC-AT systems	O 3.3 V		
SPI_MOSI	A95	Data out from module to carrier board SPI BIOS flash	O 3.3 VSB	PU 4K75 3.3 VSB	
SMB_ALERT#	B15	System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system.	I 3.3 VSB	PU 100 k $\Omega$ 3.3 VSB	
BIOS_DIS0#	A34	Selection strap to determine the BIOS boot device	I 3.3 VSB	PU 10 k $\Omega$ 3.3 VSB	
BIOS_DIS1#	B88	Selection strap to determine the BIOS boot device	I 3.3 VSB	PU 10 k $\Omega$ 3.3 VSB	
DDI1_CTRLDATA_AUX-	D16	Multiplexed with DP1_AUX- and HDMI1_CTRLDATA		PU 100 k $\Omega$ 3.3 V	
DP1_AUX-		DP AUX- function if DDI1_DDC_AUX_SEL is no connect	I/O PCIE		
HDMI1_CTRLDATA		HDMI/DVI I2C CTRLDATA if DDI1_DDC_AUX_SEL is pulled high	I/O OD 3.3 V		
DDI2_CTRLDATA_AUX-	C33	Multiplexed with DP2_AUX- and HDMI2_CTRLDATA.		PU 100 k $\Omega$ 3.3 V	
DP2_AUX-		DP AUX- function if DDI2_DDC_AUX_SEL is no connect	I/O PCIE		
HDMI2_CTRLDATA		HDMI/DVI I2C CTRLDATA if DDI2_DDC_AUX_SEL is pulled high	I/O OD 3.3 V		
DDI3_CTRLDATA_AUX-	C37	Multiplexed with DP3_AUX- and HDMI3_CTRLDATA.		PU 100 k $\Omega$ 3.3 V	
DP3_AUX-		DP AUX- function if DDI3_DDC_AUX_SEL is no connect	I/O PCIE		
HDMI3_CTRLDATA		HDMI/DVI I2C CTRLDATA if DDI3_DDC_AUX_SEL is pulled high	I/O OD 3.3 V		



### Caution

1. The signals listed in the table above are used as chipset configuration straps during system reset. In this condition (during reset), they are inputs that are pulled to the correct state by either COM Express™ internally implemented resistors or chipset internally implemented resistors that are located on the module.
2. No external DC loads or external pull-up or pull-down resistors should change the configuration of the signals listed in the above table. External resistors may override the internal strap states and cause the COM Express™ module to malfunction and/or cause irreparable damage to the module.

# 9 System Resources

## 9.1 I/O Address Assignment

The I/O address assignment of the conga-TC570 module is functionally identical with a standard PC/AT.



### Note

*The BIOS assigns PCI and PCI Express I/O resources from FFF0h downwards. Non PnP/PCI/PCI Express compliant devices must not consume I/O resources in that area.*

### 9.1.1 LPC Bus

On the conga-TC570 the PCI Express Bus acts as the subtractive decoding agent. All I/O cycles that are not positively decoded are forwarded to the PCI Bus not the ESPI or LPC Bus. Only specified I/O ranges are forwarded to the ESPI/LPC Bus. In the congatec Embedded BIOS the following I/O address ranges are sent to the ESPI/LPC Bus:

2Eh – 2Fh

4Eh – 4Fh

60h, 64h

8Ch – 8Dh (consumed internally by ESPI to LPC bridge)

A00h – A1Fh

E00h - EFFh (always used internally)

Parts of these ranges are not available if a Super I/O is used on the carrier board. If a Super I/O is not implemented on the carrier board, then these ranges are available for customer use. If you require additional LPC Bus resources other than those mentioned above, or need more information about this subject, contact congatec technical support for assistance.

## 9.2 PCI Configuration Space Map

Bus Number (hex)	Device Number (hex)	Function Number (hex)	Description
00h	00h	00h	HOST and DRAM Controller
00h	02h	00h	Integrated Graphics Device
00h	04h	00h	Dynamic Tuning Technology
00h	06h	00h	PEG60
00h	08h	00h	Gaussian Mixture Model and Neural Network Accelerator
00h	12h	00h	Thermal Subsystem
00h	0Ah	00h	Crash-log SRAM
00h	0Ah	05h	Host Bridge PCIE
00h	14h	00h	USB 3.0 xHCI Controller
00h	14h	02h	RAM Controller
00h ( Note1)	16h	00h	Management Engine (ME) Interface 1
00h ( Note1)	16h	01h	Intel ME Interface 2
00h ( Note1)	16h	02h	ME IDE Redirection (IDE-R) Interface
00h ( Note1)	16h	03h	ME Keyboard and Text (KT) Redirection
00h ( Note1)	16h	04h	Intel ME Interface 3
00h ( Note1)	16h	05h	Intel ME Interface 4
00h	17h	00h	SATA Controller
00h	1Ch	00h	Not connected (PCI Express Root Port)
00h (Note2)	1Ch	04h	PCI Express Root Port 5
00h (Note2)	1Ch	05h	PCI Express Root Port 6
00h (Note2)	1Ch	06h	PCI Express Root Port 7
00h (Note2)	1Ch	07h	PCI Express Root Port 8
00h (Note2)	1Dh	00h	PCI Express Root Port 9 connected to Ethernet controller
00h (Note2)	1Dh	01h	PCI Express Root Port 10
00h (Note2)	1Dh	04h	PCI Express Root Port 13
00h (Note2)	1Dh	03h	PCI Express Root Port 12
00h (Note2)	1Dh	02h	PCI Express Root Port 11
00h (Note2)	1Ch	02h	PCI Express Root Port 3
00h	1Fh	00h	PCI to ESPI Bridge
00h	1Fh	03h	Intel® High Definition Audio
00h	1Fh	04h	SMBus Controller
00h	1Fh	05h	SPI Flash Controller
01h (Note3)	00h	00h	PCIe Device connected to PEG Root Port 6:0
02h (Note3)	00h	00h	PCIe Device inserted in PCI Express Port 7
03h (Note3)	00h	00h	PCIe Device inserted in PCI Express Port 0
04h (Note3)	00h	00h	PCIe Device inserted in PCI Express Port 1
05h (Note3)	00h	00h	PCIe Device inserted in PCI Express Port 2

06h (Note3)	00h	00h	PCIe Device inserted in PCI Express Port 3
07h (Note3)	00h	00h	Intel Ethernet controller I225
08h (Note3)	00h	00h	PCIe Device inserted in PCI Express Port 4
09h (Note3)	00h	00h	PCIe Device inserted in PCI Express Port 5
0Ah (Note3)	00h	00h	PCIe Device inserted in PCI Express Port 6



#### Note

1. In the standard configuration, the Intel Management Engine (ME) related devices are partly present or not present at all.
2. The PCI Express Ports are visible only if a device is attached to the PCI Express Slot on the carrier board.
3. The Table represents a case when a Single function PCI/PCIe device is connected to all possible slots on the carrier board. The given bus numbers will change based on actual hardware configuration.



#### Note

Internal PCI devices not connected to the conga-TC570 are not listed.

## 9.3 I<sup>2</sup>C

Onboard resources are not connected to the I<sup>2</sup>C bus. Address 16h is reserved for congatec Battery Management solutions.

## 9.4 SM Bus

System Management (SM) bus signals are connected to the Intel® chipset. The SM bus is not intended to be used by off-board non-system management devices. For more information about this subject contact congatec technical support.

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## 10 BIOS Setup Description

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The BIOS setup description of the conga-TC570 can be viewed without having access to the module. However, access to the restricted area of the congatec website is required in order to download the necessary tool (CgMlfViewer) and Menu Layout File (MLF).

The MLF contains the BIOS setup description of a particular BIOS revision. The MLF can be viewed with the CgMlfViewer tool. This tool offers a search function to quickly check for supported BIOS features. It also shows where each feature can be found in the BIOS setup menu.

For more information, read the application note "AN42 - BIOS Setup Description" available at [www.congatec.com](http://www.congatec.com).



### Note

*If you do not have access to the restricted area of the congatec website, contact your local congatec sales representative.*

### 10.1 Navigating the BIOS Setup Menu

The BIOS setup menu shows the features and options supported in the congatec BIOS. To access and navigate the BIOS setup menu, press the <DEL> or <F2> key during POST. The right frame displays the key legend. Above the key legend is an area reserved for text messages. These text messages explain the options and the possible impacts when changing the selected option in the left frame.

### 10.2 BIOS Versions

The BIOS displays the BIOS project name and the revision code during POST, and on the main setup screen. The initial production BIOS for conga-TC570 is identified as BVTLR1xx or BUTLR1xx, where:

- R is the identifier for a BIOS ROM file,
- 1 is the so called feature number and
- xx is the major and minor revision number.

The binary size for BVTL and BUTL is 32 MB.

## 10.3 Updating the BIOS

BIOS updates are recommended to correct platform issues or enhance the feature set of the module. The conga-TC570 features a congatec/AMI AptioEFI firmware on an onboard flash ROM chip. You can update the firmware with the congatec System Utility. The utility has five versions—UEFI shell, DOS based command line<sup>1</sup>, Win32 command line, Win32 GUI, and Linux version.

For more information about “Updating the BIOS” refer to the user’s guide for the congatec System Utility “CGUTLm1x.pdf” on the congatec website at [www.congatec.com](http://www.congatec.com).



### Note

<sup>1</sup>. *Deprecated*



### Caution

*The DOS command line tool is not officially supported by congatec and therefore not recommended for critical tasks such as firmware updates. We recommend to use only the UEFI shell for critical updates.*

### 10.3.1 Update from External Flash

For instructions on how to update the BIOS from external flash, refer to the AN7\_External\_BIOS\_Update.pdf application note on the congatec website at <http://www.congatec.com>.

## 10.4 Supported Flash Devices

The conga-TC570 supports:

- Macronix MX25L25645G (32 MB)

The flash device can be used on the carrier board to support external BIOS. For more information about external BIOS support, refer to the Application Note “AN7\_External\_BIOS\_Update.pdf” on the congatec website at <http://www.congatec.com>.