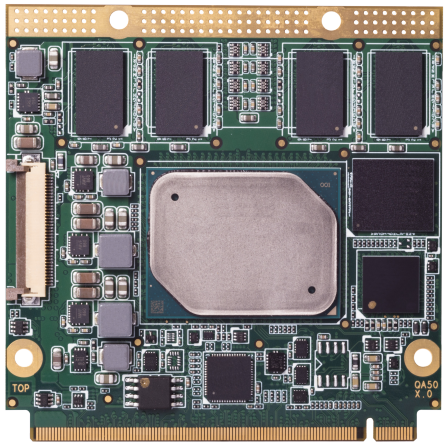

Qseven® conga-QA5

Qseven module based on the Intel® Atom®, Pentium® and Celeron® Apollo Lake SoC

User's Guide

Revision 1.9

congatec

Revision History

Revision	Date (yyyy.mm.dd)	Author	Changes
0.1	2017.03.06	BEU	• Preliminary release
1.0	2017.09.14	BEU	• Minor improvements throughout the document • Updated peripheral interfaces in section 2.1 "Feature List", supported OS in section 2.2 "Supported Operating Systems" and supported features in section 6.3.4 "OEM BIOS Code/Data" • Added power consumption values in section 2.5 "Power Consumption" and 2.6 "Supply Voltage Battery Power" • Updated table 16 "USB Signal Descriptions", table 17 "SDIO Signal Descriptions", table 21 " HDMI/DVI Signal Descriptions", table 22 "LPC Signal Descriptions", and table 28 "Miscellaneous Signal Descriptions" • Added inrush current in section 5.12 "Power Control" • Added section 5.15 "MIPI CSI-2" • Added information to section 9 "System Resources" • Added information to section 10 "BIOS Setup Description"
1.1	2018.06.25	BEU	• Added an errata as a document to read in the preface section. • Updated "Electrostatic Sensitive Device" information on page 3. • Removed Android from supported OS in section 2.2 "Supported Operating Systems" • Edited the USB configurations in section 3 "Block Diagram" • Correct values in table 5 "Power Consumption Values" • Corrected footnote symbols in table 33 "PCI Configuration Space Map" • Updated security features in table 3 "Feature Summary" and section 6.6 "Security Features" • Added EFT caution to section 5.4 "USB" • Updated section 5.5 "UART" • Added information about USB_ID in table 16 "USB Signal Descriptions"
1.2	2018.08.21	BEU	• Added new variant 015513 to table 2 "conga-QA5 (Industrial Variants)"
1.3	2019.04.12	BEU	• Removed part numbers in section 4 "Cooling Solutions" • Added new commercial variant 015524 to table 1 and table 5
1.4	2019.05.29	BEU	• Added power consumption values of new variant 015524 to table 5 • Updated note in section 4 "Cooling Solutions" • Updated supported flash device to W25Q64JVSSIG in section 10.4 "Supported Flash Devices"
1.5	2019.09.19	BEU	• Updated recommended torque and added table 7 in section 4 "Cooling Solutions" • Updated supported OS for CGUTIL and added caution in section 10.3 "Updating the BIOS" • Updated supported flash device to W25Q64JVSSIQ in section 10.4 "Supported Flash Devices"
1.6	2020.01.07	BEU	• Corrected table reference in section 5.5 "UART" • Updated reference to power supply design guide in section 5.12 "Power Control" • Updated section 6.1 "eMMC 5.0" • Added note about min. pulse width to several button signals in table 27 and 28 • Added reference to BIOS Setup Description application note in section 10 "BIOS Setup Description" • Updated section 11 "Industry Specifications"
1.7	2021.02.19	BEU	• Updated the note in section 5.5 "UART" • Corrected the storage temperature for industrial variants in section 2.7 “Environmental Specifications”

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1.8	2021.04.15	BEU	• Updated display interfaces in table 1, 2, 3, 12, 22, 29 and section 3 "Block Diagram", 5.8 "Display Interfaces", 5.8.1 "DP++ Port" • Deleted section 5.8.2 "HDMI", 5.8.3 "DVI", 11 "Industry Specifications"
1.9	2021.07.06	BEU	• Updated congatec AG to congatec GmbH throughout the document • Added Software License Information to preface section • Updated section 6.4 "congatec Battery Management Interface"

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Preface

This user's guide provides information about the components, features, connector and BIOS Setup menus available on the conga-QA5. It is one of four documents that should be referred to when designing a Qseven® application. This user's guide should be read in conjunction with the document "Errata_congatec_xA5_designs". Click on the document name to download it.

The other reference documents that should be used include the following:

Qseven® Design Guide
Qseven® Specification

The links to these documents can be found on the congatec GmbH website at www.congatec.com

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Terminology

Term	Description
PCIe	Peripheral Component Interface Express – next-generation high speed Serialized I/O bus
PCI Express Lane	One PCI Express Lane is a set of 4 signals that contains two differential lines for Transmitter and two differential lines for Receiver. Clocking information is embedded into the data stream.
x1, x2, x4, x8, x16	x1 refers to one PCI Express Lane of basic bandwidth; x2 to a collection of two PCI Express Lanes; etc.. Also referred to as x1, x2, x4, x8, or x16 link.
eMMC	Embedded MultiMediaCard
SD card	Secure Digital card is a non-volatile memory card format developed for use in portable devices.
USB	Universal Serial Bus
SATA	Serial AT Attachment: serial-interface standard for hard disks
HDA	High Definition Audio
DDI	Digital Display Interface
DP	DisplayPort is a VESA open digital communications interface.
TMDS	Transition Minimized Differential Signaling
LPC	Low Pin-Count is a low speed interface used for peripheral circuits such as Super I/O controllers, which typically combine legacy device support into a single IC.
I²C Bus	Inter-Integrated Circuit Bus is a simple two-wire bus with a software-defined protocol that was developed to provide the communications link between integrated circuits in a system.
SM Bus	System Management Bus is a popular derivative of the I²C-bus.
SPI Bus	Serial Peripheral Interface is a synchronous serial data link standard that operates in full duplex mode.
GbE	Gigabit Ethernet
LVDS	Low-Voltage Differential Signaling
DDC	Display Data Channel is an I²C bus interface between a display and a graphics adapter.
N.C.	Not connected
N.A.	Not available
T.B.D.	To be determined

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1 Introduction

1.1 Qseven® Concept

The Qseven® concept is an off-the-shelf, multi vendor, Single-Board-Computer that integrates all the core components of a common PC and is mounted onto an application specific carrier board. Qseven® modules have a standardized form factor of 70mm x 70mm and a specified pinout based on the high speed MXM system connector. The pinout remains the same regardless of the vendor. The Qseven® module provides the functional requirements for an embedded application. These functions include, but are not limited to, graphics, sound, mass storage, network interface and multiple USB ports.

A single ruggedized MXM connector provides the carrier board interface to carry all the I/O signals to and from the Qseven® module. This MXM connector is a well known and proven high speed signal interface connector that is commonly used for high speed PCI Express graphics cards in notebooks.

Carrier board designers can use as little or as many of the I/O interfaces as deemed necessary. The carrier board can therefore provide all the interface connectors required to attach the system to the application specific peripherals. This versatility allows the designer to create a dense and optimized package, which results in a more reliable product while simplifying system integration.

The Qseven® evaluation carrier board provides carrier board designers with a reference design platform and the opportunity to test all the Qseven® I/O interfaces available and then choose what are suitable for their application. Qseven® applications are scalable, which means once a carrier board has been created there is the ability to diversify the product range through the use of different performance class Qseven® modules. Simply unplug one module and replace it with another, no need to redesign the carrier board.

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1.2 conga-QA5 Options Information

The conga-QA5 is available in eleven variants. This user's guide describes all of these variants and the table below shows the different configurations available. Check for the Part No. that applies to your product. This will tell you what options described in this user's guide are available on your particular module.

Table 1 conga-QA5 (Commercial Variants)

Part-No	015500	015501	015502	015503	015522	015523
Processor	Intel® Atom® E3950 1.6 GHz Quad Core	Intel® Atom® E3940 1.6 GHz Quad Core	Intel® Atom® E3930 1.3 GHz Dual Core	Intel® Atom® E3950 1.6 GHz Quad Core	Intel® Celeron® N3350 1.1 GHz Dual Core	Intel® Pentium® N4200 1.1 GHz Quad Core
CPU Burst Freq.	2.0 GHz	1.8 GHz	1.8 GHz	2.0 GHz	2.4 GHz	2.5 GHz
L2 Cache	2 MB	2 MB	2 MB	2MB	2 MB	2 MB
Onboard Memory	8 GB 1866 MT/s DDR3L	4 GB 1866 MT/s DDR3L	2 GB 1866 MT/s DDR3L	4 GB 1866 MT/s DDR3L	4 GB 1866 MT/s DDR3L	8 GB 1866 MT/s DDR3L
Graphics	Intel® HD Graphics 505	Intel® HD Graphics 500	Intel® HD Graphics 500	Intel® HD Graphics 505	Intel® HD Graphics 500	Intel® HD Graphics 505
GFX Normal/Burst	500 / 650 MHz	400 / 600 MHz	400 / 550 MHz	500 / 650 MHz	200 / 650 MHz	200 / 750 MHz
LVDS/eDP	LVDS	LVDS	LVDS	LVDS	LVDS	LVDS
Default USB Configuration	1x USB3.0 / 2.0 5x USB2.0	1x USB3.0 / 2.0 5x USB2.0	1x USB3.0 / 2.0 5x USB2.0	1x USB3.0 / 2.0 5x USB2.0	1x USB3.0 / 2.0 5x USB2.0	1x USB3.0 / 2.0 5x USB2.0
DDI	DP++	DP++	DP++	DP++	DP++	DP++
eMMC	32 GB	16 GB	8 GB	16 GB	16 GB	32 GB
Ethernet Controller	Intel® I211	Intel® I211	Intel® I211	Intel® I211	Intel® I211	Intel® I211
SOC TDP	12 W	9.5 W	6.5 W	12 W	6 W	6 W

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Part-No	015524
Processor	Intel® Celeron® J3455 1.5 GHz Quad Core
CPU Burst Freq.	2.5 GHz
L2 Cache	2 MB
Onboard Memory	4 GB 1866 MT/s DDR3L
Graphics	Intel® HD Graphics 500
GFX Normal/Burst	250 / 750 MHz
LVDS/eDP	LVDS
Default USB Configuration	1x USB3.0 / 2.0 5x USB2.0
DDI	DP++
eMMC	16 GB
Ethernet Controller	Intel® I211
SOC TDP	10 W

Table 2 conga-QA5 (Industrial Variants)

Part-No	015510	015511	015512	015513
Intel Processor	Intel® Atom® E3950 1.6 GHz Quad Core	Intel® Atom® E3940 1.6 GHz Quad Core	Intel® Atom® E3930 1.3 GHz Dual Core	Intel® Atom® E3950 1.6 GHz Quad Core
CPU Burst Freq.	2.0 GHz	1.8 GHz	1.8 GHz	2.0 GHz
L2 Cache	2 MB	2 MB	2 MB	2 MB
Onboard Memory	8 GB 1866 MT/s DDR3L	4 GB 1866 MT/s DDR3L	2 GB 1866 MT/s DDR3L	8 GB 1866 MT/s DDR3L
Graphics	Intel® HD Graphics 505	Intel® HD Graphics 500	Intel® HD Graphics 500	Intel® HD Graphics 505
GFX Normal/Burst	500 / 650 MHz	400 / 600 MHz	400 / 550 MHz	500 / 650 MHz
LVDS/eDP 1.3	LVDS	LVDS	LVDS	eDP 1.3
Default USB Configuration	1x USB3.0/2.0 5x USB2.0	1x USB3.0/2.0 5x USB2.0	1x USB3.0/2.0 5x USB2.0	1x USB3.0/2.0 5x USB2.0
DDI	DP++	DP++	DP++	DP++
eMMC	32 GB	16 GB	8 GB	32 GB
Ethernet Controller	Intel® I210	Intel® I210	Intel® I210	Intel® I210
SOC TDP	12 W	9.5 W	6.5 W	12 W

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2 Specifications

2.1 Feature List

Table 3 Feature Summary

Form Factor	Based on Qseven® form factor specification revision 2.0	
Processor	Based on full industrial Intel® Atom® and commercial Pentium®/Celeron® Apollo Lake Architecture	
Memory	Single or dual channel non-ECC DDR3L onboard memory interface with up to 8 GB system memory and data rates up to 1866 MT/s	
Chipset	Integrated in the SoC	
Onboard Storage	eMMC 5.0 onboard flash up to 64 GB	
Audio	Intel® High Definition Audio and Integrated Audio DSP with Intel® Smart Sound Technology	
Ethernet	Onboard Intel® Ethernet Controller I211 (Commercial Variants) or I210 (Industrial Variants) connected via one PCI Express® x1 link by default	
Graphics Interfaces	Intel® HD Graphics Gen9-LP supporting DirectX12, OpenGL 4.3, OpenGL ES 3.0, OpenCL 1.2, full HW acceleration for HEVC(H2.65), H.264, MVC, VP8, VP9, MPEG2, VC-1, WMV9 and JPEG/MJPEG	
	1x LVDS (default) or eDP interface (assembly option)*1 1x Dedicated DDI and 1x Optional DDI (assembly option)*2 with support for DP++*3	**NOTE**: *1 *Either eDP or LVDS signals supported. Both signals are not supported. Only variant 015513 provides eDP by default.* *2 *Variants equipped with the optional DDI interface do not support LVDS.* *3 *The conga-QA5 does not natively support TMDS. A DP++ to TMDS converter (e.g. PTN3360D) needs to be implemented.*
Peripheral Interfaces	2x SATA 6Gb/s Up to 4x PCI Express® Gen2 x1 links without LAN (requires custom BIOS) USB Interfaces: - 1x USB 3.0/2.0 + 5x USB 2.0 (default) or - 2x USB 3.0/2.0 + 2x USB 2.0 or - 8x USB 2.0	SD (MMC not supported) UART SPI Bus LPC Bus I²C Bus
BIOS Features	AMI Aptio® UEFI 5.x firmware; 8 MByte serial SPI with congatec Embedded BIOS features (OEM Logo, OEM CMOS Defaults, LCD Control, Display Auto Detection, Backlight Control, Flash Update)	
Power Mgmt	ACPI 5.0 compliant with battery support. Also supports Suspend to RAM (S3).	
congatec Board Controller	Multi Stage Watchdog, non-volatile User Data Storage, Manufacturing and Board Information, Board Statistics, BIOS Setup Data Backup, I²C bus (fast mode, 400 kHz, multi-master), Power Loss Control	
Security	Integrated Intel® PTT (TPM 2.0). Infineon SLB9665 (LPC TPM 2.0) or SLB9660 (LPC TPM 1.2) available by assembly option.	

Note

Some of the features mentioned in the above Feature Summary are optional. Check the article number of your module and compare it to the option information list on page 11 of this user's guide to determine what options are available on your particular module.

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2.2 Supported Operating Systems

The conga-QA5 supports the following operating systems:

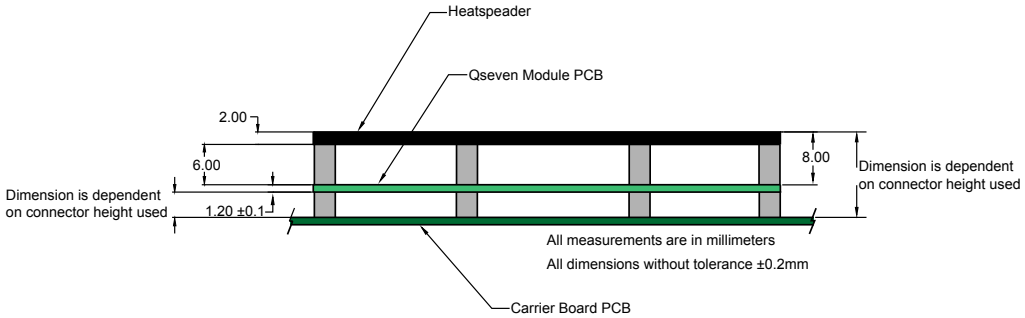
- Microsoft® Windows® 10 Enterprise (64-bit)
- Microsoft® Windows® 10 IoT Core (32/64-bit)
- Linux 3.x/4.x
- Yocto 2.x

Note

For the installation of Microsoft® Windows® 10 (64-bit), congatec GmbH recommends a minimum storage capacity of 20 GB. congatec will not offer technical support for systems with less than 20 GB storage space.

2.3 Mechanical Dimensions

- 70.0 mm x 70.0 mm
- The Qseven™ module, including the heatspreader plate, PCB thickness and bottom components, is up to approximately 12mm thick.



Rear View of Qseven Module

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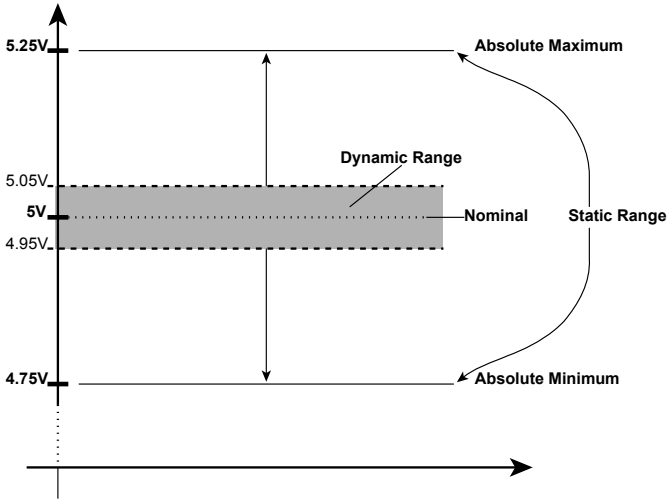
2.4 Supply Voltage Standard Power

- 5V DC ± 5%

The dynamic range shall not exceed the static range.



2.4.1 Electrical Characteristics

Characteristics			Min.	Typ.	Max.	Units	Comment
5V	Voltage	± 5%	4.75	5.00	5.25	Vdc	
	Ripple		-	-	± 50	mV_{PP}	0-20MHz
	Current						
5V_SB	Voltage	± 5%	4.75	5.00	5.25	Vdc	
	Ripple				± 50	mV_{PP}	

2.4.2 Rise Time

The input voltages shall rise from 10% of nominal to 90% of nominal at a minimum slope of 250V/s. The smooth turn-on requires that, during the 10% to 90% portion of the rise time, the slope of the turn-on waveform must be positive.

Note

For information about the input power sequencing of the Qseven® module, refer to the Qseven® specification.

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2.5 Power Consumption

The power consumption values were measured with the following setup:

- conga-QA5 COM
- modified congatec carrier board
- conga-QA5 cooling solution
- Microsoft Windows® 10 (64-bit)

Note

The CPU was stressed to its maximum workload with the Intel® Thermal Analysis Tool.

The power consumption values were recorded during the following system states:

Table 4 Measurement Description

System State	Description	Comment
S0: Minimum value	Lowest frequency mode (LFM) with minimum core voltage during desktop idle.	
S0: Maximum value	Highest frequency mode (HFM/Turbo Boost).	The CPU was stressed to its maximum frequency.
S0: Peak value	Highest current spike during the measurement of "S0: Maximum value". This state shows the peak value during runtime.	Consider this value when designing the system's power supply to ensure that sufficient power is supplied during worst case scenarios.
S3	COM is powered by VCC_5V_SBY.	
S5	COM is powered by VCC_5V_SBY.	

Note

1. *The fan and SATA drives were powered externally.*
2. *All other peripherals except the LCD monitor were disconnected before measurement.*

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The tables below provide additional information about the power consumption data for each of the conga-QA5 variants offered. The values are recorded at various operating modes.

Table 5 Power Consumption Values

Part No.	Memory Size	H.W Rev.	BIOS Rev.	OS (64-bit)	CPU			Current (A) @ 5V				
					Variant	Cores	Base / Burst Freq. (GHz)	S0: Min	S0: Max	S0: Peak	S3	S5
015500	8 GB	A.1	QA50R015	Windows 10	Atom® E3950	4	1.6 / 2.0	0.26	4.36	4.78	0.08	0.04
015501	4 GB	A.1	QA50R015	Windows 10	Atom® E3940	4	1.6 / 1.8	0.22	2.92	3.10	0.06	0.04
015502	2 GB	A.1	QA50R015	Windows 10	Atom® E3930	2	1.3 / 1.8	0.22	2.10	2.26	0.06	0.04
015503*	4 GB	A.1	QA50R015	Windows 10	Atom® E3950	4	1.6 / 2.0	0.26	4.36	4.78	0.08	0.04
015522	4 GB	A.1	QA50R015	Windows 10	Celeron® N3350	2	1.1 / 2.4	0.24	2.44	3.56	0.06	0.04
015523	8 GB	A.1	QA50R015	Windows 10	Pentium® N4200	4	1.1 / 2.5	0.26	2.70	4.40	0.10	0.06
015224	4 GB	B.0	QA50R145	Windows 10	Celeron® J3455	4	1.5 / 2.3	0.30	3.42	4.90	0.06	0.05
015510*	8 GB	A.1	QA50R015	Windows 10	Atom® E3950	4	1.6 / 2.0	0.26	4.36	4.78	0.08	0.04
015511*	4 GB	A.1	QA50R015	Windows 10	Atom® E3940	4	1.6 / 1.8	0.22	2.92	3.10	0.06	0.04
015512*	2 GB	A.1	QA50R015	Windows 10	Atom® E3930	2	1.3 / 1.8	0.22	2.10	2.26	0.06	0.04
015513*	8 GB	A.1	QA50R015	Windows 10	Atom® E3950	4	1.6 / 2.0	0.26	4.36	4.78	0.08	0.04

Note

With fast input voltage rise time, the inrush current may exceed the measured peak current.

** Because the power consumption of module variants with the same CPU are similar (maxmimum ± 5%), we measured only one variant. The power consumption values for the other variants were copied.*

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2.6 Supply Voltage Battery Power

Table 6 CMOS Battery Power Consumption

RTC @	Voltage	Current
-10°C	3V DC	1.89 µA
20°C	3V DC	2.06 µA
70°C	3V DC	2.98 µA

Note

1. *Do not use the CMOS battery power consumption values listed above to calculate CMOS battery lifetime.*
2. *Measure the CMOS battery power consumption in your customer specific application in worst case conditions (for example, during high temperature and high battery voltage).*
3. *Consider also the self-discharge of the battery when calculating the lifetime of the CMOS battery. For more information, refer to application note AN9_RTC_Battery_Lifetime.pdf on congatec GmbH website at www.congatec.com/support/application-notes.*
4. *We recommend to always have a CMOS battery present when operating the conga-QA5.*

2.7 Environmental Specifications

Temperature (commercial variants)	Operation:	0° to 60°C	Storage: -20° to +80°C
Temperature (industrial variants)	Operation:	-40° to 85°C	Storage: -40° to +85°C
Humidity	Operation:	10% to 90%	Storage: 5% to 95%

Caution

The above operating temperatures must be strictly adhered to at all times. When using a congatec heatspreader, the maximum operating temperature refers to any measurable spot on the heatspreader's surface.

Humidity specifications are for non-condensing conditions.

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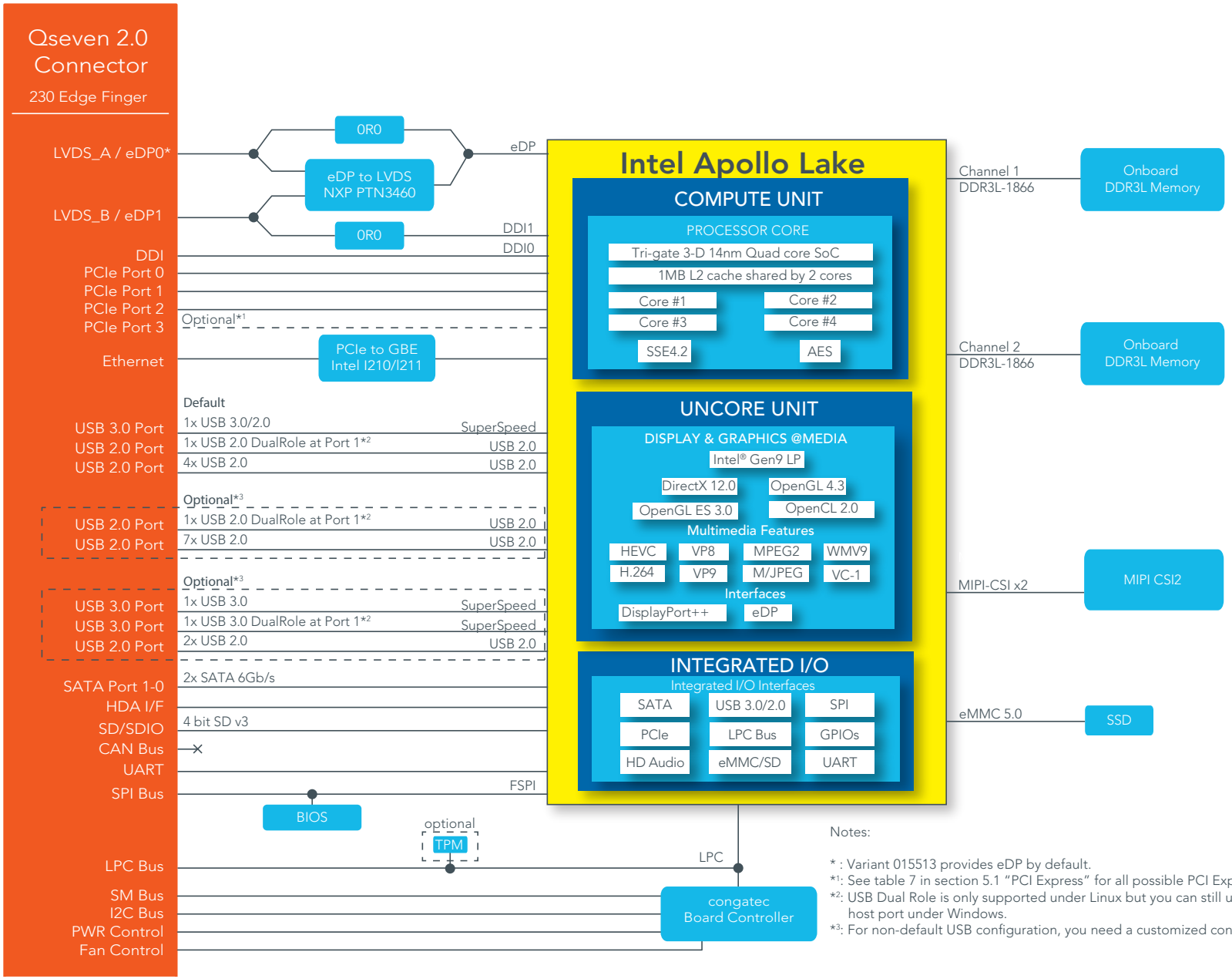
3 Block Diagram



Notes:

* : Variant 015513 provides eDP by default.
*1: See table 7 in section 5.1 "PCI Express" for all possible PCI Express configurations.
*2: USB Dual Role is only supported under Linux but you can still use this port a standard USB host port under Windows.
*3: For non-default USB configuration, you need a customized conga-QA5 variant.

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4 Cooling Solutions

congatec GmbH offers the cooling solutions listed in Table 7 for conga-QA5. The dimensions of the cooling solutions are shown in the sub-sections. All measurements are in millimeters.

Table 7 Cooling Solution Variants

	Cooling Solution	Part No	Description
1	HSP	015533	Heatspreader with 2.7 mm bore-hole standoffs for lidded CPU Intel Atom CPU variants
		015532	Heatspreader with M2.5 mm threaded standoffs for lidded Intel Atom CPU variants
		015537	Heatspreader with 2.7 mm bore-hole standoffs for bare-die Intel Pentium and Celeron CPU variants
		015536	Heatspreader with M2.5 mm threaded standoffs for bare-die Intel Pentium and Celeron CPU variants
2	CSP	015531	Passive cooling with 2.7 mm bore-hole standoffs for lidded Intel Atom CPU variants
		015530	Passive cooling with M2.5 mm threaded standoffs for lidded Intel Atom CPU variants
		015535	Passive cooling with 2.7 mm bore-hole standoffs for bare-die Intel Pentium and Celeron CPU variants
		015534	Passive cooling with M2.5 mm threaded standoffs for bare-die Intel Pentium and Celeron CPU variants

Note

1. *We recommend a maximum torque of 0.4 Nm for the mounting screws and to start with the two screws furthest from the CPU die.*

2. *The gap pad material used on congatec heatspreaders may contain silicon oil that can seep out over time depending on the environmental conditions it is subjected to. For more information about this subject, contact your local congatec sales representative and request the gap pad material manufacturer's specification.*

Caution

1. *The congatec heatspreaders/cooling solutions are tested only within the commercial temperature range of 0° to 60°C. Therefore, if your application that features a congatec heatspreader/cooling solution operates outside this temperature range, ensure the correct operating temperature of the module is maintained at all times. This may require additional cooling components for your final application's thermal solution.*

2. *For adequate heat dissipation, use the mounting holes on the cooling solution to attach it to the module. Apply thread-locking fluid on the screws if the cooling solution is used in a high shock and/or vibration environment. To prevent the standoff from stripping or cross-threading, use non-threaded carrier board standoffs to mount threaded cooling solutions.*

3. *For applications that require vertically-mounted cooling solution, use only coolers that secure the thermal stacks with fixing post. Without the fixing post feature, the thermal stacks may move.*

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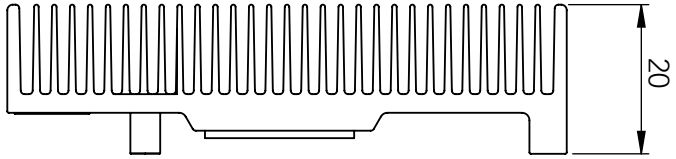
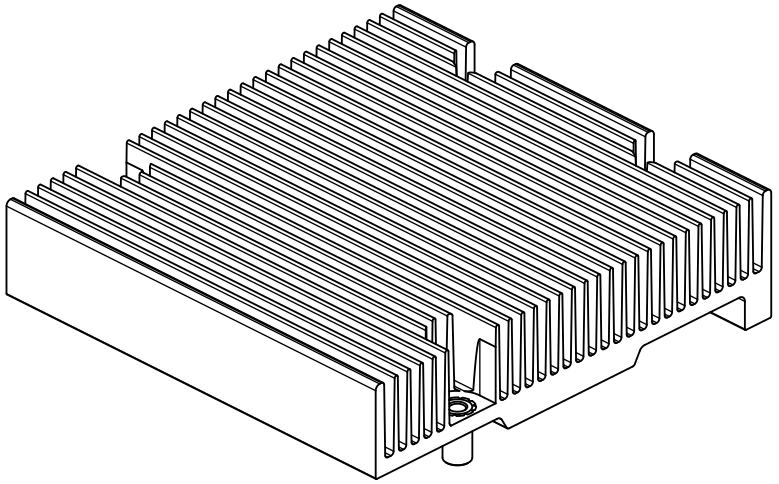
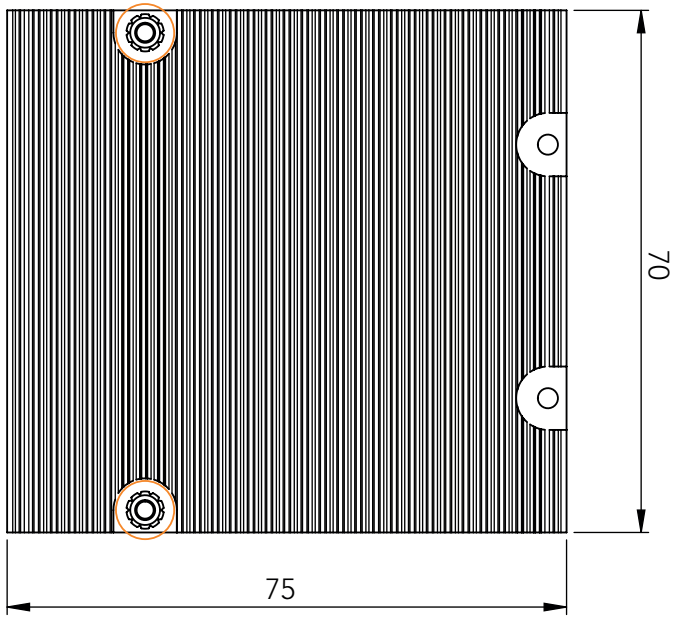
4.1 CSP Dimensions

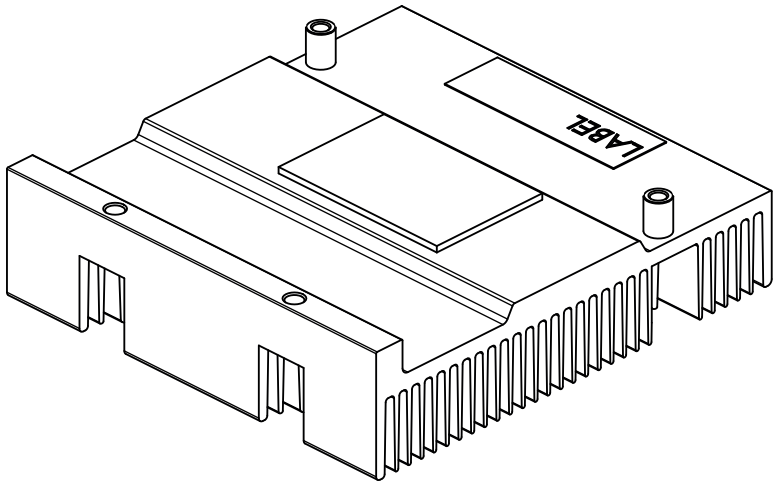
For Lidded Variants





M2.5 x 8 mm threaded standoff for threaded version
or
ø2.7 x 8 mm non-threaded standoff for borehole version





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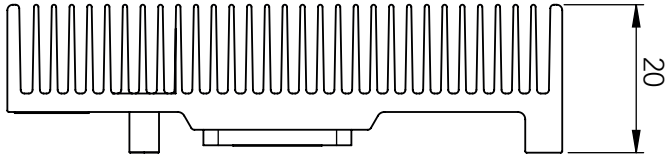
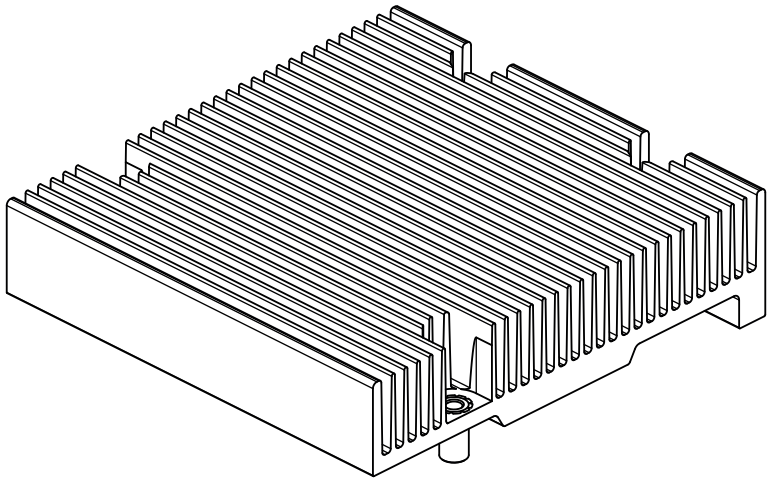
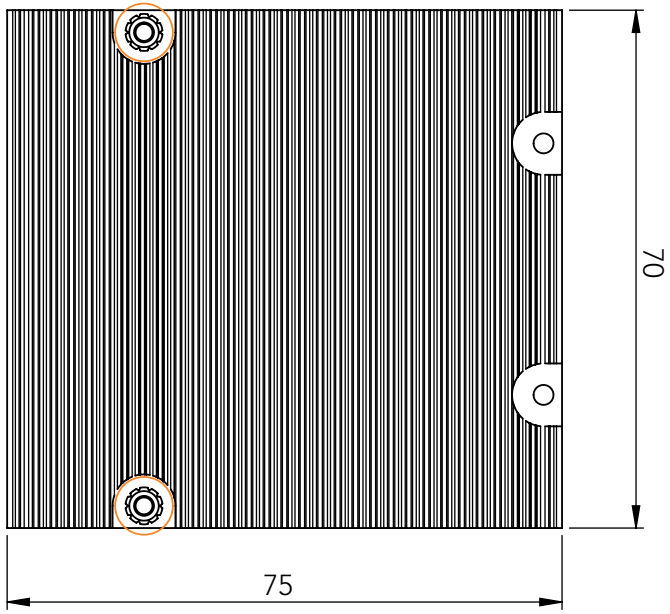
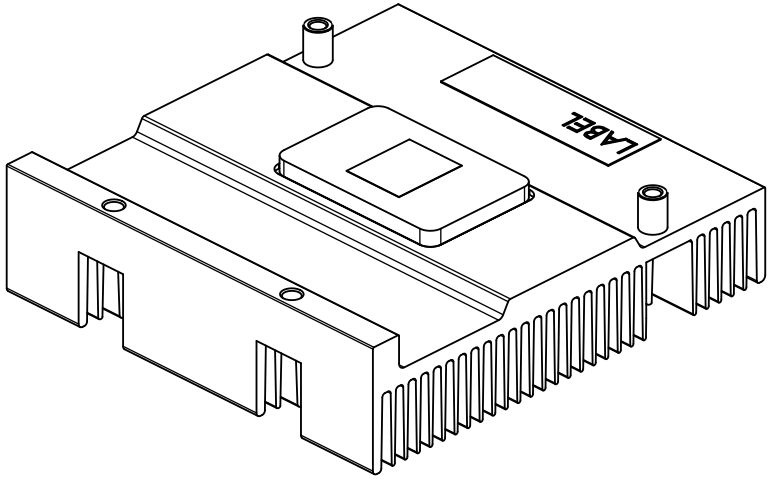
For Bare-die Variants





M2.5 x 8 mm threaded standoff for threaded version
or
ø2.7 x 8 mm non-threaded standoff for borehole version





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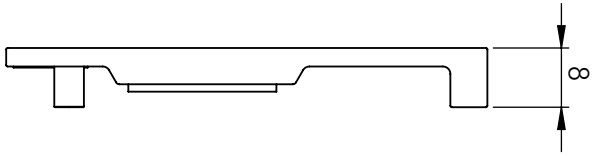
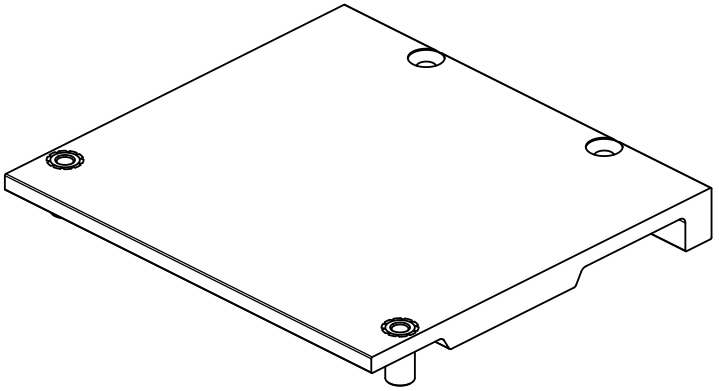
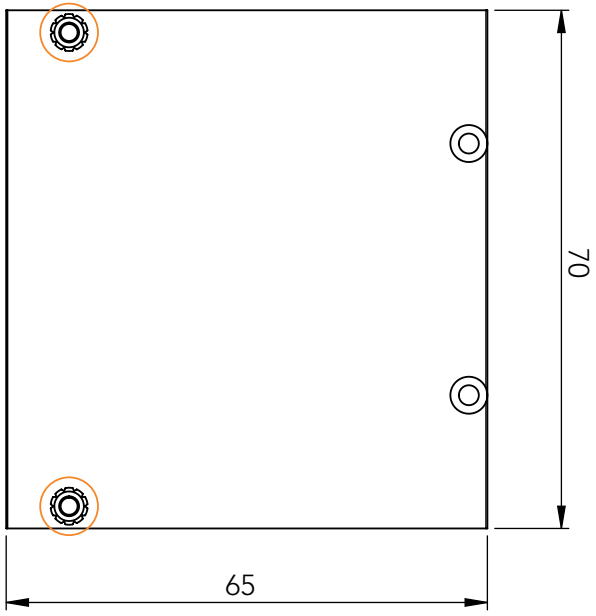
4.2 Heatspreader Dimensions

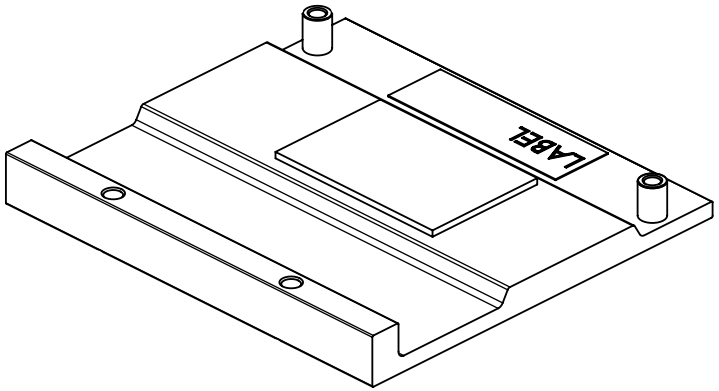
For Lidded Variants





M2.5 x 8 mm threaded standoff for threaded version
or
ø2.7 x 8 mm non-threaded standoff for borehole version





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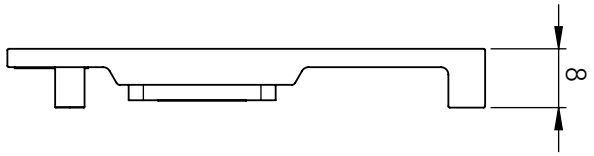
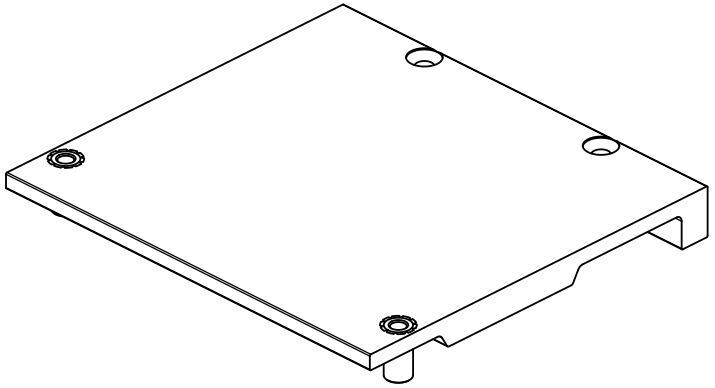
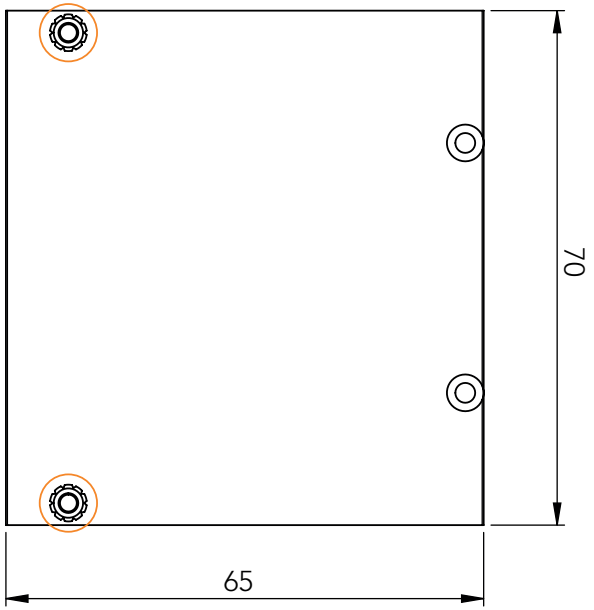
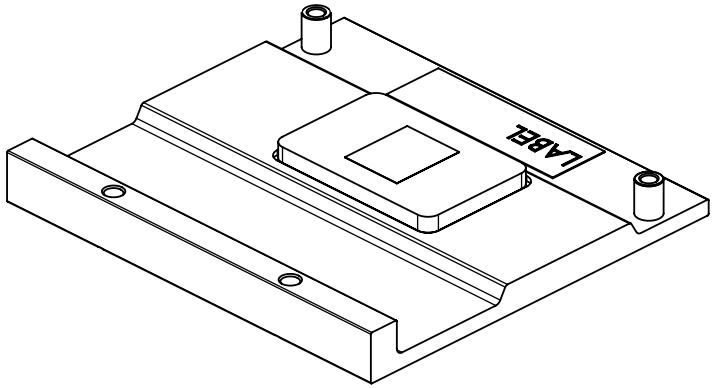
For Bare-die variants





M2.5 x 8 mm threaded standoff for threaded version
or
ø2.7 x 8 mm non-threaded standoff for borehole version





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5 Connector Subsystems

The conga-QA5 is based on the Qseven® standard and therefore has 115 edge fingers on the top and bottom side of the module that mate with the 230-pin card-edge MXM connector located on the carrier board. This connector is able to interface the available signals of the conga-QA5 with the carrier board peripherals.

5.1 PCI Express™

The conga-QA5 offers up to four PCIe lanes externally on the Edge finger. The lanes are Gen 2 compliant and offer support for full 5 Gb/s bandwidth in each direction per x1 link. Default configuration for the lanes is 3 x1 link. Other configurations are possible as shown in the table below but require a customized BIOS firmware. Contact congatec technical support for more information.

The PCI Express interface is based on the PCI Express Specification 2.0 with Gen 1 (2.5 Gb/s) and Gen 2 (5 Gb/s) speed. For more information, refer to the conga-QA5 pinout table in section 8 “Signal Descriptions and Pinout Tables”.

Table 8 PCI Express™ Options

	x1	x2	x4	Gigabit Ethernet
Default	3			Yes
Option		2		Yes
Option			1	Yes
Option	2	1		Yes
Option	4			No

Note

The options require a customized BIOS.

5.2 Gigabit Ethernet

The conga-QA5 offers a Gigabit Ethernet interface on the edge finger via the onboard Intel® I211 (Commercial Vairants) or I210 (Industrial Variants) Gigabit Ethernet controller. This controller is connected to the SoC through the fourth PCI Express lane by default. The Ethernet interface consists of 4 pairs of low voltage differential pair signals designated from GBE0_MD0± to GBE0_MD3± plus control signals for link activity indicators. These signals can be routed to a 10/100/1000 BaseT RJ45 connector with integrated or external isolation magnetics on the carrier board.

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5.3 SATA

The conga-QA5 offers two 6Gb/s SATA interfaces on the edge finger via a SATA host controller integrated in the SoC. The SATA host controller supports DMA auto-activate feature, hot-plug detect, AHCI operations and data transfer rates up to 6Gb/s. IDE Mode is not supported.

5.4 USB

The conga-QA5 offers up to eight USB ports routed directly from the SoC as shown below:

Table 9 USB Options

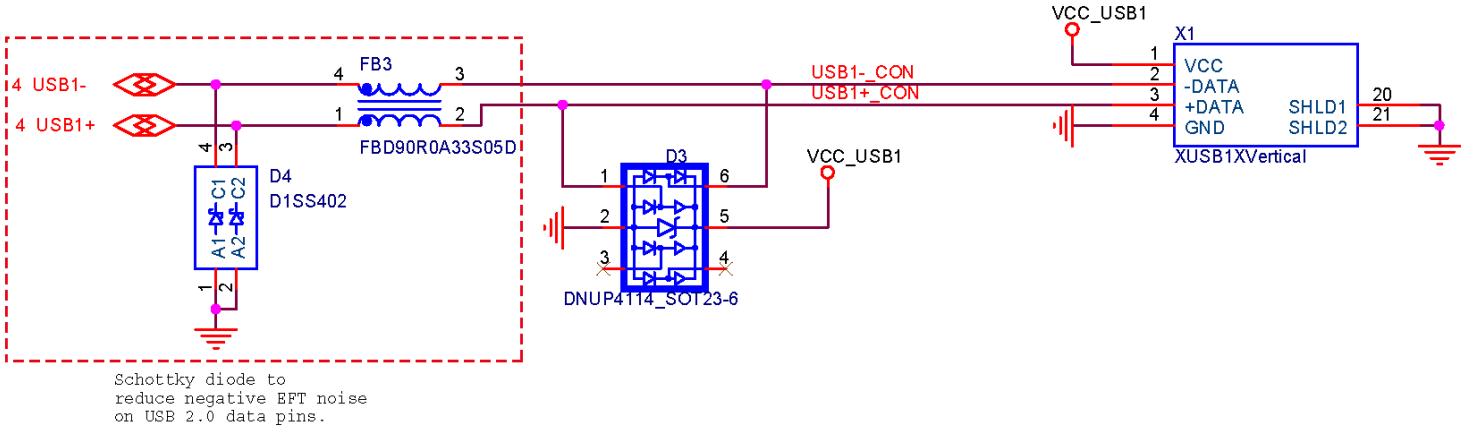
	USB 2.0	USB 2.0 Dual Role	USB 3.0	USB 3.0 Dual Role
Default	4	1	1	
Option	7	1		
Option	2		1	1

Note

USB Dual Role is only supported under Linux. The port is a standard USB Host port under Windows. For non-default USB configuration, you need a customized conga-QA5 variant.

Caution

To pass the Electrical Fast Transient (EFT) test, you must add a schottky diode (1SS402 or equivalent) to all USB2.0 data lanes routed to a connector on your carrier board. The schottky diode must be placed before the common-mode choke as shown below.



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5.5 UART

The conga-QA5 provides one UART port routed from the SoC by default. Optionally, the UART port can be routed from the congatec board controller (cBC) instead. For more information, see Table 14 "UART Signal Descriptions".

Note

The validated Intel HSUART driver and the congatec Board Controller UART driver is available on the congatec website at www.congatec.com.

5.6 SD Card

The conga-QA5 offers a 4-bit SD interface connected to the SD v3.01 host controller integrated in the SoC. It supports up to 50 MHz 3.3V signalling and up to 208 Mhz 1.8V signalling. The MMC standard is not supported.

5.7 High Definition Audio (HDA)

The conga-QA5 provides a High Definition Audio interface connected to the audio controller in the SoC and supports one HDA audio codec.

5.8 Display Interfaces

The conga-QA5 offers up to three independent displays as shown in the table below:

Table 10 Display Combination

	Display 1		Display 2		Display 3	
	External	Max. Resolution	Internal/External	Max. Resolution	Internal/External	Max. Resolution
Default	DP	4096x2160 @ 60Hz	LVDS (up to 2x 24 bit)	1920x1200 @ 60Hz (dual channel mode)	N/A	N/A
Option	DP	4096x2160 @ 60Hz	eDP	3840x2160 @ 60Hz	N/A	N/A
Option	DP	4096x2160 @ 60Hz	eDP	3840x2160 @ 60Hz	DP	4096x2160 @ 60Hz

Note

For non-default display configuration, you need a customized conga-QA5 variant.

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5.8.1 DP++ Port

DisplayPort is an open, industry standard digital display interface, that has been developed within the Video Electronics Standards Association (VESA). The DisplayPort specification defines a scalable digital display interface with optional audio and content protection capability. It defines a license-free, royalty-free, state-of-the-art digital audio/video interconnect, intended to be used primarily between a computer and its display monitor.

Note

See table 9 above for possible display combinations.

5.8.2 LVDS / eDP

The conga-QA5 offers an LVDS interface on the edge finger. The interface is provided by routing the onboard PTN3460 eDP to LVDS bridge to the eDP port of the SoC. The bridge processes the incoming DisplayPort stream, converts the DP protocol to LVDS protocol and transmits the processed stream in LVDS format.

The LVDS interface supports:

- single or dual channel LVDS interface (color depths of 18 bpp or 24 bpp)
- integrated flat panel interface with clock frequency up to 112 MHz
- VESA standard or JEIDA data mapping
- automatic panel detection via Embedded Panel Interface based on VESA EDID™ 1.3
- resolution up to 1920x1200 in dual channel LVDS mode

The LVDS/eDP pins on the Qseven® connector provide LVDS signals by default, but can optionally support eDP signals (assembly option). Only the variant 015513 provides eDP by default. For more information, contact congatec technical support.

Note

The LVDS/eDP interface supports either LVDS or eDP signals. Both signals are not supported simultaneously. See table 9 above for possible display combinations.

5.9 LPC

The conga-QA5 offers the Low Pin Count (LPC) bus. The LPC bus is similar to a serialized ISA bus but with fewer signals. Due to the software compatibility with the ISA bus, it is easy to implement I/O extensions such as additional serial ports on an application specific baseboard using the LPC bus. Many devices are available for this cost-efficient, low-speed interface designed to support low bandwidth and legacy devices.

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Note

The LPC clock frequency is 25 MHz. The LPC_DRQ# signal is not supported. The SERIRQ# signal is programmable to operate with the cBC. See table 8 above for possible display combinations.

5.10 SPI

The module integrates a 64 MBit SPI Flash device for the UEFI BIOS. Optionally, the on-module SPI Flash can be disabled and a carrier board-based 3V 64 Mbit SPI Flash device with SFDP feature (e.g. W25Q64FVSSIG) can be utilized to boot the module.

5.11 I²C Bus

The I²C bus is provided by the congatec board controller. The bus has 2.2k ohm pull-ups resistors on the CLK and DATA signals and is powered from runtime 3.3V.

5.12 Power Control

The conga-QA5 supports ATX-style power supplies control. In order to do this the power supply must provide a constant source of VCC_5V_SB power. The AT-style power supply (5V only) is also supported. In this case, the conga-QA5's pin PWRBTN# should be left unconnected, pin SUS_S3# should control the main power regulators on the carrier board (+3.3V...) and pins VCC_5V_SB should be connected to the 5V input power rail according to the Qseven specification.

PWGIN

PWGIN (pin 26) can be connected to an external power good circuit. This input is optional and should be left unconnected when not used. Through the use of an internal monitor on the +5V input voltage and/or the internal power supplies, the conga-QA5 module is capable of generating its own power good.

SUS_S3#

The SUS_S3# (pin 18) signal is an active-low output that can be used to control the main 5V rail of the power supply for module and all other main power supplies on carrier board. In order to accomplish this, the signal must be inverted with an inverter/transistor that is supplied by standby voltage (ATX-style) or system input voltage (AT-style) and is located on the carrier board.

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PWRBTN#

When using ATX-style power supplies PWRBTN# (pin 20) is used to connect to a momentary-contact, active-low debounced push-button input while the other terminal on the push-button must be connected to ground. This signal is internally pulled up to 3.3V_SB using a 10k resistor. When PWRBTN# is asserted, it indicates that an operator wants to turn the power on or off. The response to this signal from the system may vary as a result of modifications made in BIOS settings or by system software.

Power Supply Implementation Guidelines

5V input power is the sole operational power source for the conga-QA5. The remaining necessary voltages are internally generated on the module using onboard voltage regulators. A carrier board designer should be aware of the following important information when designing a power supply for a conga-QA5 application:

- It has also been noticed that on some occasions, problems occur when using a 5V power supply that produces non monotonic voltage when powered up. The problem is that some internal circuits on the module (e.g. clock-generator chips) will generate their own reset signals when the supply voltage exceeds a certain voltage threshold. A voltage dip after passing this threshold may lead to these circuits becoming confused resulting in a malfunction. It must be mentioned that this problem is quite rare but has been observed in some mobile power supply applications. The best way to ensure that this problem is not encountered is to observe the power supply rise waveform through the use of an oscilloscope to determine if the rise is indeed monotonic and does not have any dips. This should be done during the power supply qualification phase therefore ensuring that the above mentioned problem does not arise in the application. For more information, see the "Power Supply Design Guide for Desktop Platform Form Factors" document at www.intel.com.

Inrush and Maximum Current Peaks on VCC_5V_SB and VCC

The inrush current on the conga-QA5 VCC_5V_SB power rail can go up as high as 7.10A and as high as 16.4A on the conga-QA5 VCC power rail within a short time (approx 100µs) and with a voltage rise time of 100µs. Sufficient decoupling capacitance must be implemented to ensure proper power-up sequencing.

5.13 Power Management

The conga-QA5 complies with the Advanced Configuration and Power Interface Specification Revision 5.0.

5.14 SMBus

The SMBus is provided by the congatec board controller. The bus is powered by standby 3.3V and has 2.2k ohm pull-ups resistors on the CLK and DATA signals. The ALERT# signal has 10K-ohm pull-up resistor. Optionally, the SMBus can be connected to the SoC SMBus via an isolation switch controlled through BIOS.

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5.15 MIPI CSI-2

The MIPI CSI-2 connector is available as an option for high-volume projects. It requires a specific software implementation—depending on the operating system and camera application. Contact your local sales representative for further details.

The flip-lock actuator of the MIPI CSI-2 connector is fragile and must be handled with care.

Follow these steps to attach the flat-foil cable to the MIPI CSI-2 connector:

1. Remove the cooling solution (if installed).
2. Gently press against both sides of the actuator from below to flip the actuator open.
3. Fully slide the flat-foil cable inside the slot below the actuator. The exposed conductive traces of the flat-foil cable must face up.
4. Gently press against both sides of the actuator from above until the actuator is firmly locked.
5. Install the cooling solution.

Follow these steps to remove the flat-foil cable from the MIPI CSI-2 connector:

1. Remove the cooling solution (if installed).
2. Gently press against both sides of the actuator from below to flip the actuator open.
3. Carefully remove the flat-foil cable.
4. Install the cooling solution.

Caution

Do not try to pull the flat-foil connector out without removing the cooling solution and opening the actuator first. Also, do not use pressure to open the actuator by more than 45°. Otherwise, the connector will be damaged.

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6 Additional Features

6.1 eMMC 5.0

The conga-QA5 offers an optional eMMC 5.0 flash onboard with up to 64 GB capacity. Changes to the onboard eMMC may occur during the lifespan of the module in order to keep up with the rapidly changing eMMC technology. The performance of the newer eMMC may vary depending on the eMMC technology.

Note

For adequate operation of the eMMC, ensure that at least 15 % of the eMMC storage is reserved for vendor-specific functions.

6.2 congatec Board Controller (cBC)

The conga-QA5 is equipped with a Texas Instruments Tiva™ TM4E1231H6ZRBI microcontroller. This onboard microcontroller plays an important role for most of the congatec BIOS features. It fully isolates some of the embedded features such as system monitoring or the I²C bus from the x86 core architecture, which results in higher embedded feature performance and more reliability, even when the x86 processor is in a low power mode.

6.2.1 Board Information

The cBC provides a rich data-set of manufacturing and board information such as serial number, EAN number, hardware and firmware revisions, and so on. It also keeps track of dynamically changing data like runtime meter and boot counter.

6.2.2 Fan Control

The conga-QA5 has additional signals and functions to further improve system management. One of these signals is an output signal called FAN_PWMOUT that allows system fan control using a PWM (Pulse Width Modulation) output. Additionally, there is an input signal called FAN_TACHOIN that provides the ability to monitor the system's fan RPMs (revolutions per minute). This signal must receive two pulses per revolution in order to produce an accurate reading. For this reason, a two pulse per revolution fan or similar hardware solution is recommended.

6.2.3 Power Loss Control

The cBC has full control of the power-up of the module and therefore can be used to specify the behavior of the system after an AC power loss condition. Supported modes are "Always On", "Remain Off" and "Last State".

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6.2.4 Watchdog

The conga-QA5 is equipped with a multi stage watchdog solution that can be triggered by software of external hardware. For more information about the watchdog feature, see the BIOS setup description of this document and the application note AN3_Watchdog.pdf on the congatec GmbH website at www.congatec.com.

6.3 OEM BIOS Customization

The conga-QA5 is equipped with congatec Embedded BIOS, which is based on American Megatrends Inc. Aptio UEFI firmware. The congatec Embedded BIOS allows system designers to modify the BIOS. For more information about customizing the congatec Embedded BIOS, refer to the congatec System Utility user's guide CGUTLm1x.pdf on the congatec website at www.congatec.com or contact technical support.

The customization features supported are described below:

6.3.1 OEM Default Settings

This feature allows system designers to create and store their own BIOS default configuration. Customized BIOS development by congatec for OEM default settings is no longer necessary because customers can easily perform this configuration by themselves using the congatec system utility CGUTIL. See congatec application note AN8_Create_OEM_Default_Map.pdf on the congatec website for details on how to add OEM default settings to the congatec Embedded BIOS.

6.3.2 OEM Boot Logo

This feature allows system designers to replace the standard text output displayed during POST with their own BIOS boot logo. Customized BIOS development by congatec for OEM Boot Logo is no longer necessary because customers can easily perform this configuration by themselves using the congatec system utility CGUTIL. See congatec application note AN8_Create_And_Add_Bootlogo.pdf on the congatec website for details on how to add OEM boot logo to the congatec Embedded BIOS.

6.3.3 OEM POST Logo

This feature allows system designers to replace the congatec POST logo displayed in the upper left corner of the screen during BIOS POST with their own BIOS POST logo. Use the congatec system utility CGUTIL 1.5.4 or later to replace/add the OEM POST logo.

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6.3.4 OEM BIOS Code/Data

With the congatec embedded BIOS it is possible for system designers to add their own code to the BIOS POST process. The congatec Embedded BIOS first calls the OEM code before handing over control to the OS loader.

Except for custom specific code, this feature can also be used to support verb tables for HDA codecs, PCI/PCIe opROMs, bootloaders, rare graphic modes and Super I/O controller initialization.

Note

The OEM BIOS code of the new UEFI based firmware is only called when the CSM (Compatibility Support Module) is enabled in the BIOS setup menu. Contact congatec technical support for more information on how to add OEM code.

6.3.5 OEM DXE Driver

This feature allows designers to add their own UEFI DXE driver to the congatec embedded BIOS. Contact congatec technical support for more information on how to add an OEM DXE driver.

6.4 congatec Battery Management Interface

In order to facilitate the development of battery powered mobile systems based on embedded modules, congatec has defined an interface for the exchange of data between a x86 CPU module (using an ACPI operating system) and a Smart Battery system. A system developed according to the congatec Battery Management Interface Specification can provide the battery management functions supported by an ACPI capable operating system (e.g. charge state of the battery, information about the battery, alarms/events for certain battery states, ...) without the need for any additional modifications to the system BIOS.

In addition to the ACPI-compliant Control Method Battery mentioned above, the latest versions of the conga-QA7 BIOS and board controller firmware also support the LTC1760 battery manager from Linear Technology and a battery only solution (no charger). All three battery solutions are supported on the I2C bus and the SMBus. This gives the system designer more flexibility when choosing the appropriate battery sub-system.

For more information about the supported Battery Management Interface contact your local congatec sales representative.

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6.5 API Support (CGOS)

In order to benefit from the above mentioned non-industry standard feature set, congatec provides an API that allows application software developers to easily integrate all these features into their code. The CGOS API (congatec Operating System Application Programming Interface) is the congatec proprietary API that is available for all commonly used Operating Systems such as Win32, Win64, Linux. The architecture of the CGOS API driver provides the ability to write application software that runs unmodified on all congatec CPU modules. All the hardware related code is contained within the congatec embedded BIOS on the module. See section 1.1 of the CGOS API software developers guide, which is available on the congatec website.

6.6 Security Features

The conga-QA5 has an integrated Intel® PTT (TPM 2.0). Additionally, an Infineon SLB9665 (LPC TPM 2.0) or SLB9660 (LPC TPM 1.2) is available by assembly option.

Note

You can enable/disable the integrated Intel® PTT (TPM 2.0) in BIOS Setup: Enter BIOS Setup (see section 10.1 "Navigating the BIOS Setup Menu"), navigate to "Advanced Setup" and then "Platform Trust Technology". Always disable fTPM if you use an external TPM.

6.7 Suspend to RAM

The Suspend to RAM feature is available on the conga-QA5.

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7 conga Tech Notes

The conga-QA5 has some technological features that require additional explanation. The following section will give the reader a better understanding of some of these features. This information will also help to gain a better understanding of the information found in the system resources section of this user's guide as well as some of the setup nodes found in the BIOS Setup Program description section.

7.1 Intel Apollo Lake SoC Features

7.1.1 Processor Core

Some of the features supported by the Intel® Apollo Lake SoC are:

- Dual/Quad Core Processor
  - 2 modules of 2 cores each (Quad Core Processor)
  - Supporting Out of Order Execution (OOE)
  - Enhanced Intel SpeedStep® Technology
  - Intel® 64 bit Architecture
- Intel® full virtualization architecture supports
  - Intel® VT-x with Extended Page Tables (EPT)
  - Intel® Virtualization Technology for Directed I/O (VT-d)
- Thermal management support via Intel® Thermal Monitor (TM1 and TM2)

Note

Intel® Hyper-Threading technology is not supported (four cores execute four threads).

7.1.1.1 Intel Virtualization Technology

Intel® Virtualization Technology (Intel® VT) makes a single system appear as multiple independent systems to software. This allows multiple, independent operating systems to run simultaneously on a single system. Intel® VT comprises technology components to support virtualization of platforms based on Intel architecture microprocessors and chipsets. Intel® Virtualization Technology for IA-32, Intel® 64 and Intel® Architecture Intel® VT-x) added hardware support in the processor to improve the virtualization performance and robustness.

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Note

congatec does not offer virtual machine monitor (VMM) software. All VMM software support questions and queries should be directed to the VMM software vendor and not congatec technical support.

7.1.1.2 AHCI

The Apollo Lake SoC provides hardware support for Advanced Host Controller Interface (AHCI), a programming interface for SATA host controllers. Platforms supporting AHCI may take advantage of performance features such as no master/slave designation for SATA devices (each device is treated as a master) and hardware-assisted native command queuing. AHCI also provides usability enhancements such as Hot-Plug.

7.1.1.3 Thermal Management

ACPI is responsible for allowing the operating system to play an important part in the system's thermal management. This results in the operating system having the ability to take control of the operating environment by implementing cooling decisions according to the demands put on the CPU by the application.

The conga-QA5 ACPI thermal solution offers two different cooling policies.

- **Passive Cooling**

When the temperature in the thermal zone must be reduced, the operating system can decrease the power consumption of the processor by throttling the processor clock. One of the advantages of this cooling policy is that passive cooling devices (in this case the processor) do not produce any noise. Use the "passive cooling trip point" setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to start or stop the passive cooling procedure.

- **Critical Trip Point**

If the temperature in the thermal zone reaches a critical point then the operating system will perform a system shut down in an orderly fashion in order to ensure that there is no damage done to the system as result of high temperatures. Use the "critical trip point" setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to shut down the system.

Note

The end user must determine the cooling preferences for the system by using the setup nodes in the BIOS setup program to establish the appropriate trip points.

If passive cooling is activated and the processor temperature is above the trip point the processor clock is throttled. See section 12 of the ACPI Specification 2.0 C for more information about passive cooling.

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7.2 ACPI Suspend Modes and Resume Events

conga-QA5 supports S3 (STR= Suspend to RAM). For more information about S3 wake events see section 10.4.6 “ACPI Configuration Submenu”.

S4 (Suspend to Disk) is not supported by the BIOS (S4_BIOS) but it is supported by the following operating systems (S4_OS= Hibernate):

- Windows® 10 and Linux

This table lists the “Wake Events” that resume the system from S3 unless otherwise stated in the “Conditions/Remarks” column:

Wake Event	Conditions/Remarks
Power Button	Wakes unconditionally from S3-S5.
Onboard LAN Event	Device driver must be configured for Wake On LAN support.
PCI Express WAKE#	Wakes unconditionally from S3-S5.
PME#	Activate the wake up capabilities of a PCI device using Windows Device Manager configuration options for this device OR set Resume On PME# to Enabled in the Power setup menu.
USB Mouse/Keyboard Event	When Standby mode is set to S3, USB Hardware must be powered by standby power source. Set USB Device Wakeup from S3/S4 to ENABLED in the ACPI setup menu (if setup node is available in BIOS setup program). In Device Manager look for the keyboard/mouse devices. Go to the Power Management tab and check ‘Allow this device to bring the computer out of standby’.
RTC Alarm	Activate and configure Resume On RTC Alarm in the Power setup menu. Only available in S5.
Watchdog Power Button Event	Wakes unconditionally from S3-S5.

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8 Signal Descriptions and Pinout Tables

The following section describes the signals found on Qseven® module's edge fingers.

Table 2 describes the terminology used in this section for the Signal Description tables. The PU/PD column indicates if a pull-up or pull-down resistor has been used, if the field entry area in this column for the signal is empty, then no pull-up or pull-down resistor has been implemented. The "#" symbol at the end of the signal name indicates that the active or asserted state occurs when the signal is at a low voltage level. When "#" is not present, the signal is asserted when at a high voltage level.

Note

Not all the signals described in this section are available on all conga-QA5 variants. Use the article number of the module and refer to the options table in section 1 to determine the options available on the module.

Table 11 Signal Tables Terminology Descriptions

Term	Description
I	Input Pin
O	Output Pin
OC	Open Collector Output Pin
OD	Open Drain Output Pin
PP	Push Pull Output Pin
I/O	Bi-directional Input/Output Pin
P	Power Input Pin
NA	Not applicable
NC	Not Connected
PCIE	PCI Express differential pair signals. In compliance with the PCI Express Base Specification 2.0
GB_LAN	Gigabit Ethernet Media Dependent Interface differential pair signals. In compliance with IEEE 802.3ab 1000Base-T Gigabit Ethernet Specification.
USB	Universal Serial Bus differential pair signals. In compliance with the Universal Serial Bus Specification 2.0
SATA	Serial Advanced Technology Attachment differential pair signals. In compliance with the Serial ATA High Speed Serialized AT Attachment Specification 2.6.
SPI	Serial Peripheral Interface bus is a synchronous serial data link that operates in full duplex mode.
LVDS	Low-Voltage Differential Signaling differential pair signals. In compliance with the LVDS Owner's Manual 4.0.
TMDS	Transition Minimized Differential Signaling differential pair signals. In compliance with the Digital Visual Interface (DVI) Specification 1.0.
CMOS	Logic input or output.

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Table 12 Edge Finger Pinout

Pin	Signal	Description	Pin	Signal	Description
1	GND	Power Ground	2	GND	Power Ground
3	GBE_MDI3-	Gigabit Ethernet MDI3-	4	GBE_MDI2-	Gigabit Ethernet MDI2-
5	GBE_MDI3+	Gigabit Ethernet MDI3+	6	GBE_MDI2+	Gigabit Ethernet MDI2+
7	GBE_LINK100#	100 Mbps link speed	8	GBE_LINK1000#	1000 Mbps link speed
9	GBE_MDI1-	Gigabit Ethernet MDI1-	10	GBE_MDI0-	Gigabit Ethernet MDI0-
11	GBE_MDI1+	Gigabit Ethernet MDI1+	12	GBE_MDI0+	Gigabit Ethernet MDI0+
13	GBE_LINK#	Gigabit Ethernet Link indicator	14	GBE_ACT#	Gigabit Ethernet Activity indicator
15	GBE_CTREF (*)	Reference voltage for GBE	16	SUS_S5#	S5 (Soft OFF) – shutdown state
17	WAKE#	External system wake event	18	SUS_S3#	S3 (Suspend to RAM) – SLP
19	SUS_STAT#	Suspend status	20	PWRBTN#	Power button
21	SLP_BTN#	Sleep button	22	LID_BTN#	LID button
23	GND	Power Ground	24	GND	Power Ground
25	GND	Power Ground	26	PWGIN	Power good input
27	BATLOW#	Battery low input	28	RSTBTN#	Reset button input
29	SATA0_TX+	Serial ATA Channel 0 TX+	30	SATA1_TX+	Serial ATA Channel 1 TX+
31	SATA0_TX-	Serial ATA Channel 0 TX-	32	SATA1_TX-	Serial ATA Channel 1 TX-
33	SATA_ACT#	Serial ATA Activity	34	GND	Power Ground
35	SATA0_RX+	Serial ATA Channel 0 RX+	36	SATA1_RX+	Serial ATA Channel 1 RX+
37	SATA0_RX-	Serial ATA Channel 0 RX-	38	SATA1_RX-	Serial ATA Channel 1 RX-
39	GND	Power Ground	40	GND	Power Ground
41	BIOS_DISABLE# /BOOT_ALT#	BIOS Module disable Boot Alternative Enable	42	SDIO_CLK	SDIO Clock Output
43	SDIO_CD#	SDIO Card Detect	44	SDIO_LED	SDIO LED
45	SDIO_CMD	SDIO Command/Response	46	SDIO_WP	SDIO Write Protect
47	SDIO_PWR#	SDIO Power Enable	48	SDIO_DAT1	SDIO Data Line 1
49	SDIO_DAT0	SDIO Data Line 0	50	SDIO_DAT3	SDIO Data Line 3
51	SDIO_DAT2	SDIO Data Line 2	52	SDIO_DAT5 (*)	SDIO Data Line 5
53	SDIO_DAT4 (*)	SDIO Data Line 4	54	SDIO_DAT7 (*)	SDIO Data Line 7
55	SDIO_DAT6 (*)	SDIO Data Line 6	56	USB_DRIVE_VBUS	USB power enable pin for USB Port 1
57	GND	Power Ground	58	GND	Power Ground
59	HDA_SYNC / I2S_WS	HD Audio/AC'97 Synchronization. Multiplexed with I2S Word Select from Codec	60	SMB_CLK / GP1_I2C_CLK	SMBus Clock line. Multiplexed with General Purpose I²C bus #1 clock line
61	HDA_RST# / I2S_RST#	HD Audio/AC'97 Codec Reset. Multiplexed with I2S Codec Reset	62	SMB_DAT / GP1_I2C_DAT	SMBus Data line. Multiplexed with General Purpose I²C bus #1 data line.
63	HDA_BITCLK / I2S_CLK	HD Audio/AC'97 Serial Bit Clock. Multiplexed with I2S Serial Data Clock from Codec.	64	SMB_ALERT#	SMBus Alert input
65	HDA_SDI (**) / I2S_SDI	HD Audio/AC'97 Serial Data In. Multiplexed with I2S Serial Data Input from Codec	66	GP0_I2C_CLK	General Purpose I2C Bus No 0 clock line

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Pin	Signal	Description	Pin	Signal	Description
67	HDA_SDO / I2S_SDO	HD Audio/AC'97 Serial Data Out. Multiplexed with I2S Serial Data Output from Codec	68	GP0_I2C_DAT	General Purpose I2C Bus No 0 data line
69	THRM#	Thermal Alarm active low	70	WDTRIG#	Watchdog trigger signal
71	THRMTRIP#	Thermal Trip indicates an overheating condition	72	WDOUT	Watchdog event indicator
73	GND	Power Ground	74	GND	Power Ground
75	USB_P7- / USB_SSTX0-	USB Port 7 Differential Pair- . Multiplexed with Superspeed USB transmit differential pair-	76	USB_P6- / USB_SSRX0-	USB Port 6 Differential Pair-. Multiplexed with Superspeed USB transmit differential pair-
77	USB_P7+ / USB_SSTX0+	USB Port 7 Differential Pair+. Multiplexed with Superspeed USB transmit differential pair+	78	USB_P6+ / USB_SSRX0+	USB Port 6 Differential Pair+. Multiplexed with Superspeed USB transmit differential pair+
79	USB_6_7_OC#	Over current detect input 6/7 USB	80	USB_4_5_OC#	Over current detect input 4/5 USB
81	USB_P5- / USB_SSTX1-	USB Port 5 Differential Pair-. Multiplexed with Superspeed USB transmit differential pair-	82	USB_P4- / USB_SSRX1-	USB Port 4 Differential Pair-. Multiplexed with Superspeed USB transmit differential pair-
83	USB_P5+ / USB_SSTX1+	USB Port 5 Differential Pair+. Multiplexed with Superspeed USB transmit differential pair+	84	USB_P4+ / USB_SSRX1+	USB Port 4 Differential Pair+. Multiplexed with Superspeed USB transmit differential pair+
85	USB_2_3_OC#	Over current detect input 2/3 USB	86	USB_0_1_OC#	Over current detect input 0/1 USB
87	USB_P3-	USB Port 3 Differential Pair-	88	USB_P2-	USB Port 2 Differential Pair-
89	USB_P3+	USB Port 3 Differential Pair+	90	USB_P2+	USB Port 2 Differential Pair+
91	USB_VBUS	USB VBUS pin	92	USB_ID	USB ID pin
93	USB_P1-	USB Port 1 Differential Pair-	94	USB_P0-	USB Port 0 Differential Pair-
95	USB_P1+	USB Port 1 Differential Pair+	96	USB_P0+	USB Port 0 Differential Pair+
97	GND	Power Ground	98	GND	Power Ground
99	eDP0_TX0+ / LVDS_A0+	eDP Primary Channel 0+ LVDS Primary channel 0+	100	eDP1_TX0+ / LVDS_B0+	eDP Secondary channel 0+ LVDS Secondary channel 0+
101	eDP0_TX0- / LVDS_A0-	eDP Primary channel 0- LVDS Primary channel 0-	102	eDP1_TX0- / LVDS_B0-	eDP Secondary channel 0- LVDS Secondary channel 0-
103	eDP0_TX1+ / LVDS_A1+	eDP Primary channel 1+ LVDS Primary channel 1+	104	eDP1_TX1+ / LVDS_B1+	eDP Secondary channel 1+ LVDS Secondary channel 1+
105	eDP0_TX1- / LVDS_A1-	eDP Primary channel 1- LVDS Primary channel 1-	106	eDP1_TX1- / LVDS_B1-	eDP Secondary channel 1- LVDS Secondary channel 1-
107	eDP0_TX2+ / LVDS_A2+	eDP Primary channel 2+ LVDS Primary channel 2+	108	eDP1_TX2+ / LVDS_B2+	eDP Secondary channel 2+ LVDS Secondary channel 2+
109	eDP0_TX2- / LVDS_A2-	eDP Primary channel 2- LVDS Primary channel 2-	110	eDP1_TX2- / LVDS_B2-	eDP Secondary channel 2- LVDS Secondary channel 2-
111	LVDS_PPEN	LVDS Power enable	112	LVDS_BLEN	LVDS Backlight enable
113	eDP0_TX3+ / LVDS_A3+	eDP Primary channel 3+ LVDS Primary channel 3+	114	eDP1_TX3+ / LVDS_B3+	eDP Secondary channel 3+ LVDS Secondary channel 3+
115	eDP0_TX3- / LVDS_A3-	eDP Primary channel 3- LVDS Primary channel 3-	116	eDP1_TX3- / LVDS_B3-	eDP Secondary channel 3- LVDS Secondary channel 3-
117	GND	Power Ground	118	GND	Power Ground
119	eDP0_AUX+ / LVDS_A_CLK+	eDP Primary Auxilliary channel+ LVDS Primary channel CLK+	120	eDP1_AUX+ / LVDS_B_CLK+	eDP Secondary Auxiliary channel CLK+ LVDS Secondary channel CLK+

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Pin	Signal	Description	Pin	Signal	Description
121	eDP0_AUX- / LVDS_A_CLK-	eDP Primary Auxilliary channel- LVDS Primary channel CLK-	122	eDP1_AUX- / LVDS_B_CLK-	eDP Secondary Auxiliary channel CLK- LVDS Secondary channel CLK-
123	LVDS_BLT_CTRL / GP_PWM_OUT0	PWM Backlight brightness General Purpose PWM Output	124	GP_1-Wire_Bus (*)	General Purpose 1-wire bus interface
125	LVDS_DID_DAT / GP_I2C_DAT	DDC Display ID Data line DDC based control signal (data) for optional TMDS	126	eDP0_HPD# / LVDS_BLC_DAT	Can be used as eDP primary hotplug detect
127	LVDS_DID_CLK / GP_I2C_CLK	DDC Display ID Clock line DDC based control signal (clk) for optional TMDS	128	eDP1_HPD# / LVDS_BLC_CLK	Can be used as eDP secondary hotplug detect
129	CAN0_TX (*)	CAN TX Output for CAN Bus Channel 0	130	CAN0_RX (*)	CAN RX Input for CAN Bus Channel 0
131	DP_LANE3+ / TMDS_CLK+	DisplayPort differential pair line lane 3. Multiplexed with TMDS differential pair clock+	132	RSVD (Differential)	Reserved
133	DP_LANE3- / TMDS_CLK-	DisplayPort differential pair line lane 3. Multiplexed with TMDS differential pair clock-	134	RSVD (Differential)	Reserved
135	GND	Power Ground	136	GND	Power Ground
137	DP_LANE1+ / TMDS_LANE1+	DisplayPort differential pair line lane 1 Multiplexed with TMDS differential pair lane1	138	DP_AUX+	DisplayPort auxiliary channel
139	DP_LANE1- / TMDS_LANE1-	DisplayPort differential pair line lane 1 Multiplexed with TMDS differential pair lane1	140	DP_AUX-	DisplayPort auxiliary channel
141	GND	Power Ground	142	GND	Power Ground
143	DP_LANE2+ / TMDS_LANE0+	DisplayPort differential pair line lane 2	144	RSVD (Differential)	Reserved
145	DP_LANE2- / TMDS_LANE0-	DisplayPort differential pair line lane 2	146	RSVD (Differential)	Reserved
147	GND	Power Ground	148	GND	Power Ground
149	DP_LANE0+ / TMDS_LANE2+	DisplayPort differential pair line lane 0 Multiplexed with TMDS differential pair lane2	150	HDMI_CTRL_DAT	DDC based control signal (data) for TMDS device.
151	DP_LANE0- / TMDS_LANE2-	DisplayPort differential pair line lane 0 Multiplexed with TMDS differential pair lane2	152	HDMI_CTRL_CLK	DDC based control signal (clock) for TMDS device.
153	DP_HDMI_HPD#	Hot plug detection for TMDS	154	DP_HPD#	Hot plug detection for DP
155	PCIE_CLK_REF+	PCI Express Reference Clock+	156	PCIE_WAKE#	PCI Express Wake event
157	PCIE_CLK_REF-	PCI Express Reference Clock-	158	PCIE_RST#	Reset Signal for external devices
159	GND	Power Ground	160	GND	Power Ground
161	PCIE3_TX+	PCI Express Channel 3 Output+	162	PCIE3_RX+	PCI Express Channel 3 Input+
163	PCIE3_TX-	PCI Express Channel 3 Output-	164	PCIE3_RX-	PCI Express Channel 3 Input-
165	GND	Power Ground	166	GND	Power Ground
167	PCIE2_TX+	PCI Express Channel 2 Output+	168	PCIE2_RX+	PCI Express Channel 2 Input+
169	PCIE2_TX-	PCI Express Channel 2 Output-	170	PCIE2_RX-	PCI Express Channel 2 Input-
171	UART0_TX	Serial Data Transmitter	172	UART0_RTS#	Handshake signal, ready to receive data
173	PCIE1_TX+	PCI Express Channel 1 Output+	174	PCIE1_RX+	PCI Express Channel 1 Input+
175	PCIE1_TX-	PCI Express Channel 1 Output-	176	PCIE1_RX-	PCI Express Channel 1 Input-
177	UART0_RX	Serial Data Receiver	178	UART0_CTS#	Handshake signal, ready to send data

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Pin	Signal	Description	Pin	Signal	Description
179	PCIE0_TX+	PCI Express Channel 0 Output+	180	PCIE0_RX+	PCI Express Channel 0 Input+
181	PCIE0_TX-	PCI Express Channel 0 Output-	182	PCIE0_RX-	PCI Express Channel 0 Input-
183	GND	Power Ground	184	GND	Power Ground
185	LPC_AD0	LPC Interface Address Data 0	186	LPC_AD1	LPC Interface Address Data 1
187	LPC_AD2	LPC Interface Address Data 2	188	LPC_AD3	LPC Interface Address Data 3
189	LPC_CLK	LPC Interface Clock	190	LPC_FRAME#	LPC frame indicator
191	SERIRQ	Serialized interrupt	192	LPC_LDRQ# (*)	LPC DMA request
193	VCC_RTC	3V backup cell input	194	SPKR /GP_PWM_OUT2	Output for audio enunciator General Purpose PWM Output
195	FAN_TACHOIN	Fan tachometer input General Purpose Timer In	196	FAN_PWMOUT	Fan speed control (PWM) General Purpose PWM Output
197	GND	Power Ground	198	GND	Power Ground
199	SPI_MOSI (**)	SPI Master serial output/Slave serial input	200	SPI_CS0# (**)	SPI Chip Select 0 Output
201	SPI_MISO (**)	SPI Master serial input/Slave serial output signal	202	SPI_CS1# (*)	SPI Chip Select 1 Output
203	SPI_SCK (**)	SPI Clock Output	204	MFG_NC4	Do not connect on carrier board
205	VCC_5V_SB	+5VDC,Standby ±5%	206	VCC_5V_SB	+5VDC Standby ±5%
207	MFG_NC0	Do not connect on carrier board	208	MFG_NC2	Do not connect on carrier board
209	MFG_NC1	Do not connect on carrier board	210	MFG_NC3	Do not connect on carrier board
211	VCC	Power supply +5VDC ±5%	212	VCC	Power supply +5VDC ±5%
213	VCC	Power supply +5VDC ±5%	214	VCC	Power supply +5VDC ±5%
215	VCC	Power supply +5VDC ±5%	216	VCC	Power supply +5VDC ±5%
217	VCC	Power supply +5VDC ±5%	218	VCC	Power supply +5VDC ±5%
219	VCC	Power supply +5VDC ±5%	220	VCC	Power supply +5VDC ±5%
221	VCC	Power supply +5VDC ±5%	222	VCC	Power supply +5VDC ±5%
223	VCC	Power supply +5VDC ±5%	224	VCC	Power supply +5VDC ±5%
225	VCC	Power supply +5VDC ±5%	226	VCC	Power supply +5VDC ±5%
227	VCC	Power supply +5VDC ±5%	228	VCC	Power supply +5VDC ±5%
229	VCC	Power supply +5VDC ±5%	230	VCC	Power supply +5VDC ±5%

Note

The signals marked with asterisk symbol (*) are not supported on the conga-QA5.

On Apollo Lake SoC, the signals marked with asterisks (**) have voltage levels that are different from the levels defined in the Qseven Specification. To comply with the Qseven Specification, the signals are routed through bidirectional level shifters on the module.

The bidirectional level shifters by nature have limited driving strength. congatec therefore recommends to route these signals as short as possible. External pull up/down resistors <100k ohm are not allowed on these signals.

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Table 13 PCI Express Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
PCIE0_RX+ PCIE0_RX-	180 182	PCI Express channel 0, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE0_TX+ PCIE0_TX-	179 181	PCI Express channel 0, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE1_RX+ PCIE1_RX-	174 176	PCI Express channel 1, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 2.0.
PCIE1_TX+ PCIE1_TX-	173 175	PCI Express channel 1, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE2_RX+ PCIE2_RX-	168 170	PCI Express channel 2, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE2_TX+ PCIE2_TX-	167 169	PCI Express channel 2, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE3_RX+ PCIE3_RX-	162 164	PCI Express channel 3, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE3_TX+ PCIE3_TX-	161 163	PCI Express channel 3, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_CLK_REF+ PCIE_CLK_REF-	155 157	PCI Express Reference Clock for Lanes 0 to 3.	O PCIE		
PCIE_WAKE#	156	PCI Express Wake Event: Sideband wake signal asserted by components requesting wakeup.	I 3.3VSB	PU 10k 3.3VSB	
PCIE_RST#	158	Reset Signal for external devices.	O 3.3V		

Table 14 UART Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
UART0_TX	171	Serial Data Transmitter	O 3.3V		
UART0_RX	177	Serial Data Reciever	I 3.3V	PU 100k 3.3V	
UART0_CTS#	178	Handshake signal, ready to send data	I 3.3V	PU 100k 3.3V	
UART0_RTS#	172	Handshake signal, ready to receive data	O 3.3V		

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Table 15 Ethernet Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
GBE_MDI0+ GBE_MDI0-	12 10	Media Dependent Interface (MDI) differential pair 0. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is used for all modes.	I/O Analog		Twisted pair signals for external transformer.
GBE_MDI1+ GBE_MDI1-	11 9	Media Dependent Interface (MDI) differential pair 1. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is used for all modes.	I/O Analog		Twisted pair signals for external transformer.
GBE_MDI2+ GBE_MDI2-	6 4	Media Dependent Interface (MDI) differential pair 2. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is only used for 1000Mbit/sec Gigabit Ethernet mode.	I/O Analog		Twisted pair signals for external transformer.
GBE_MDI3+ GBE_MDI3-	5 3	Media Dependent Interface (MDI) differential pair 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is only used for 1000Mbit/sec Gigabit Ethernet mode.	I/O Analog		Twisted pair signals for external transformer.
GBE_CTREF	15	Reference voltage for carrier board Ethernet magnetics center tap. The reference voltage is determined by the requirements of the module's PHY and may be as low as 0V and as high as 3.3V. The reference voltage output should be current limited on the module. In a case in which the reference is shorted to ground, the current must be limited to 250mA or less.	REF		Not connected
GBE_LINK#	13	Ethernet controller 0 link indicator, active low.	O 3.3VSB PP		indicates only LINK100 and LINK1000
GBE_LINK100#	7	Ethernet controller 0 100Mbit/sec link indicator, active low.	O 3.3VSB PP		
GBE_LINK1000#	8	Ethernet controller 0 1000Mbit/sec link indicator, active low.	O 3.3VSB PP		
GBE_ACT#	14	Ethernet controller 0 activity indicator, active low.	O 3.3VSB PP		

Note

The conga-QA5 can drive GbE LEDs with up to 10 mA.

Table 16 SATA Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SATA0_RX+ SATA0_RX-	35 37	Serial ATA channel 0, Receive Input differential pair.	I SATA		Supports Serial ATA specification, Revision 3.1
SATA0_TX+ SATA0_TX-	29 31	Serial ATA channel 0, Transmit Output differential pair.	O SATA		Supports Serial ATA specification, Revision 3.1
SATA1_RX+ SATA1_RX-	36 38	Serial ATA channel 1, Receive Input differential pair.	I SATA		Supports Serial ATA specification, Revision 3.1
SATA1_TX+ SATA1_TX-	30 32	Serial ATA channel 1, Transmit Output differential pair.	O SATA		Supports Serial ATA specification, Revision 3.1
SATA_ACT#	33	Serial ATA Led. Open collector output pin driven during SATA command activity.	OD		up to 10mA

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Table 17 USB Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
USB_P0+ USB_P0-	96 94	Universal Serial Bus Port 0 differential pair.	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1 Can be combined with USB_SSRX0 and USB_SSTX0 signals to create a USB 3.0 port.
USB_P1+ USB_P1-	95 93	Universal Serial Bus Port 1 differential pair. This port may be optionally used as USB client port.	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1 Can be combined with USB_SSRX1 and USB_SSTX1 signals to create a USB 3.0 port.
USB_P2+ USB_P2-	90 88	Universal Serial Bus Port 2 differential pair.	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB_P3+ USB_P3-	89 87	Universal Serial Bus Port 3 differential pair.	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB_P4+ USB_P4- USB_SSRX1+ USB_SSRX1-	84 82	Universal Serial Bus Port 4 differential pair. Multiplexed with receive signal differential pairs for the Superspeed USB data path.	I/O I		USB 2.0 compliant. Backwards compatible to USB 1.1. AC coupled on module for USB_SS variant. **Note:** These pins carry either SuperSpeed or USB 2.0 signals depending on the conga-QA5 variant.
USB_P5+ USB_P5- USB_SSTX1+ USB_SSTX1-	83 81	Universal Serial Bus Port 5 differential pair. Multiplexed with transmit signal differential pairs for the Superspeed USB data path	I/O O		USB 2.0 compliant. Backwards compatible to USB 1.1. AC coupled on module for USB_SS variant. **Note:** These pins carry either SuperSpeed or USB 2.0 signals depending on the conga-QA5 variant.
USB_P6+ USB_P6- USB_SSRX0+ USB_SSRX0-	78 76	Universal Serial Bus Port 6 differential pair. Multiplexed with receive signal differential pairs for the Superspeed USB data path	I PCIE		USB 2.0 compliant. Backwards compatible to USB 1.1. AC coupled on module for USB_SS variant. **Note:** These pins carry either SuperSpeed or USB 2.0 signals depending on the conga-QA5 variant.
USB_P7+ USB_P7- USB_SSTX0+ USB_SSTX0-	77 75	Universal Serial Bus Port 7 differential pair. Multiplexed with transmit signal differential pairs for the Superspeed USB data path	O PCIE		USB 2.0 compliant. Backwards compatible to USB 1.1 AC coupled on module for USB_SS variant. **Note:** These pins carry either SuperSpeed or USB 2.0 signals depending on the conga-QA5 variant.
USB_0_1_OC#	86	Over current detect input 1. This pin is used to monitor the USB power over current of the USB Ports 0 and 1.	I 3.3VSB	PU 10k 3.3VSB	
USB_2_3_OC#	85	Over current detect input 2. This pin is used to monitor the USB power over current of the USB Ports 2 and 3.	I 3.3VSB	PU 10k 3.3VSB	
USB_4_5_OC#	80	Over current detect input 3. This pin is used to monitor the USB power over current of the USB Ports 4 and 5.	I 3.3VSB	PU 10k 3.3VSB	
USB_6_7_OC#	79	Over current detect input 4. This pin is used to monitor the USB power over current of the USB Ports 6 and 7.	I 3.3VSB	PU 10k 3.3VSB	

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USB_ID	92	USB ID pin. Configures the mode of the USB Port 1: - To use the port as a host, connect this pin to ground with a 10Ω or lower resistor. - To use the port as a client, leave the pin unconnected or connect it to ground with a 100KΩ or greater resistor. Refer to the Qseven Design guide for further details.	I 3.3VSB		Should be connected to ID pin on USB AB connector if used.
USB_VBUS	91	USB VBUS pin 5V tolerant VBUS resistance to be placed on the module VBUS capacitance to be placed on the carrier board	I 5V Passive Analog	PD 1M	
USB_DRIVE_VBUS	56	USB power enable pin for USB Port 1. Enables the power for the USB Dual role port on the carrier	O 3.3V CMOS		

Table 18 SDIO Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SDIO_CD#	43	SDIO Card Detect. This signal indicates when a SDIO/MMC card is present.	I/O 3.3V	PU 20k	
SDIO_CLK	42	SDIO Clock. With each cycle of this signal a one-bit transfer on the command and each data line occurs. This signal has maximum frequency of 48 MHz.	O 3.3V	PD 20k	
SDIO_CMD	45	SDIO Command/Response. This signal is used for card initialization and for command transfers. During initialization mode this signal is open drain. During command transfer this signal is in push-pull mode.	I/O 3.3V OD/PP	PU 20k	
SDIO_LED	44	SDIO LED. Used to drive an external LED to indicate when transfers occur on the bus.	O 3.3V		
SDIO_WP	46	SDIO Write Protect. This signal denotes the state of the write-protect tab on SD cards.	I/O 3.3V	PU 20k	
SDIO_PWR#	47	SDIO Power Enable. This signal is used to enable the power being supplied to a SD/MMC card device.	O 3.3V		
SDIO_DAT0 SDIO_DAT1 SDIO_DAT2 SDIO_DAT3 SDIO_DAT4 SDIO_DAT5 SDIO_DAT6 SDIO_DAT7	49 48 51 50 53 52 55 54	SDIO Data lines. These signals operate in push-pull mode.	I/O 3.3V OD/PP	PU 20k	Only 4-bit SDIO interface. SDIO_DAT[7:4] are not connected

Note

The conga-QA5 also supports UHS-I speed that uses I/O 1.8V.

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Table 19 HDA Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
HDA_RST#	61	HD Audio Codec Reset.	O 3.3VSB		
HDA_SYNC	59	HD Audio Serial Bus Synchronization.	O 3.3VSB		
HDA_BITCLK	63	HD Audio 24 MHz Serial Bit Clock from Codec.	O 3.3VSB		
HDA_SDO	67	HD Audio Serial Data Output to Codec.	O 3.3VSB		
HDA_SDI (**)	65	HD Audio Serial Data Input from Codec.	I 3.3VSB	PD 47k	

On Intel Apollo Lake SoC, the signals marked with asterisks (**) have voltage levels that are different from the levels defined in the Qseven Specification. To comply with the Qseven Specification, the signals are routed through bidirectional level shifters on the module.

The bidirectional level shifters by nature have limited driving strength. congatec therefore recommends to route these signals as short as possible. External pull up/down resistors <100k ohm are not allowed on these signals.

Table 20 LVDS Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
LVDS_PPEN	111	Controls panel power enable.	O 3.3V	PD 100k	
LVDS_BLEN	112	Controls panel Backlight enable.	O 3.3V	PD 100k	
LVDS_BLT_CTRL /GP_PWM_OUT0	123	Primary functionality is to control the panel backlight brightness via pulse width modulation (PWM). When not in use for this primary purpose it can be used as General Purpose PWM Output.	O 3.3V		
LVDS_A0+ LVDS_A0- eDP0_TX0+ eDP0_TX0-	99 101	LVDS primary channel differential pair 0. Display Port primary channel differential pair 0.	O LVDS/ O eDP		eDP signals are AC coupled on the module. These pins carry either LVDS or eDP signals depending on the conga-QA5 variant.
LVDS_A1+ LVDS_A1- eDP0_TX1+ eDP0_TX1-	103 105	LVDS primary channel differential pair 1. Display Port primary channel differential pair 1.	O LVDS/ O eDP		eDP signals are AC coupled on the module. These pins carry either LVDS or eDP signals depending on the conga-QA5 variant.
LVDS_A2+ LVDS_A2- eDP0_TX2+ eDP0_TX2-	107 109	LVDS primary channel differential pair 2. Display Port primary channel differential pair 2.	O LVDS/ O eDP		eDP signals are AC coupled on the module. These pins carry either LVDS or eDP signals depending on the conga-QA5 variant.

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LVDS_A3+ LVDS_A3- eDP0_TX3+ eDP0_TX3-	113 115	LVDS primary channel differential pair 3. Display Port primary channel differential pair 3.	O LVDS/ O eDP		eDP signals are AC coupled on the module. These pins carry either LVDS or eDP signals depending on the conga-QA5 variant.
LVDS_A_CLK+ LVDS_A_CLK- eDP0_AUX+ eDP0_AUX-	119 121	LVDS primary channel differential pair clock lines. Display Port primary auxiliary channel.	O LVDS/ O eDP		eDP signals are AC coupled on the module. These pins carry either LVDS or eDP signals depending on the conga-QA5 variant.
LVDS_B0+ LVDS_B0- eDP1_TX0+ eDP1_TX0-	100 102	LVDS secondary channel differential pair 0. Display Port secondary channel differential pair 0.	O LVDS/ O DP		DD1 signals are AC coupled on the module. These pins carry either LVDS or DDI1 signals depending on the conga-QA5 variant.
LVDS_B1+ LVDS_B1- eDP1_TX1+ eDP1_TX1-	104 106	LVDS secondary channel differential pair 1. Display Port secondary channel differential pair 1.	O LVDS/ O DP		DD1 signals are AC coupled on the module. These pins carry either LVDS or DDI1 signals depending on the conga-QA5 variant.
LVDS_B2+ LVDS_B2- eDP1_TX2+ eDP1_TX2-	108 110	LVDS secondary channel differential pair 2. Display Port secondary channel differential pair 2.	O LVDS/ O DP		DD1 signals are AC coupled on the module. These pins carry either LVDS or DDI1 signals depending on the conga-QA5 variant.
LVDS_B3+ LVDS_B3- eDP1_TX3+ eDP1_TX3-	114 116	LVDS secondary channel differential pair 3. Display Port secondary channel differential pair 3.	O LVDS/ O DP		DD1 signals are AC coupled on the module. These pins carry either LVDS or DDI1 signals depending on the conga-QA5 variant.
LVDS_B_CLK+ LVDS_B_CLK- eDP1_AUX+ eDP1_AUX-	120 122	LVDS secondary channel differential pair clock lines. Display Port secondary auxiliary channel.	O LVDS/ O DP		DD1 signals are AC coupled on the module. These pins carry either LVDS or DDI1 signals depending on the conga-QA5 variant.
LVDS_DID_CLK /GP2_I2C_CLK	127	Primary functionality is DisplayID DDC clock line used for LVDS flat panel detection. If primary functionality is not used it can be as General Purpose I²C bus clock line.	I/OD 3.3V	PU 2k2 3.3V	Used as DDI1_DDC_SCL for variants that do not support LVDS.
LVDS_DID_DAT /GP2_I2C_DAT	125	Primary functionality DisplayID DDC data line used for LVDS flat panel detection. If primary functionality is not used it can be as General Purpose I²C bus data line.	I/OD 3.3V	PU 2k2 3.3V	Used as DDI1_DDC_SDA for variants that do not support LVDS.
LVDS_BLC_CLK eDP1_HPD#	128	Control clock signal for external SSC clock chip. If the primary functionality is not used, it can be used as an embedded DisplayPort secondary Hotplug detection.	I/OD 3.3V	PU 10k 3.3V	Not supported on variants that provide LVDS. DDI1_HPD# for variants that do not support LVDS.
LVDS_BLC_DAT eDP0_HPD#	126	Control data signal for external SSC clock chip. If the primary functionality is not used, it can be used as an embedded DisplayPort primary Hotplug detection.	I/OD 3.3V	PU 10k 3.3V	Not supported on variants that provide LVDS. eDP_HPD# for variants that do not support LVDS.

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Table 21 DisplayPort Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
DP_LANE3+ DP_LANE3-	131 133	DisplayPort differential pair lines lane 3 (Shared with TMDS_CLK+ and TMDS_CLK-)	O DP		AC coupled on module.
DP_LANE2+ DP_LANE2-	143 145	DisplayPort differential pair lines lane 2 (Shared with TMDS_LANE0+ and TMDS_LANE0-)	O DP		AC coupled on module.
DP_LANE1+ DP_LANE1-	137 139	DisplayPort differential pair lines lane 1 (Shared with TMDS_LANE1+ and TMDS_LANE1-)	O DP		AC coupled on module.
DP_LANE0+ DP_LANE0-	149 151	DisplayPort differential pair lines lane 0 (Shared with TMDS_LANE2+ and TMDS_LANE2-)	O DP		AC coupled on module.
DP_AUX+ DP_AUX-	138 140	Auxiliary channel used for link management and device control. Differential pair lines.	I/O DP		AC coupled off module.
DP_HPD#	154	Hot plug detection signal that serves as an interrupt request.	I 3.3V	PU 10k 3.3V	Supports open drain and PushPull driver.

Note

The DisplayPort signals are shared with TMDS signals.

Table 22 TMDS Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	
TMDS_CLK+ TMDS_CLK-	131 133	TMDS differential pair clock lines. (Shared with DP_LANE3- and DP_LANE3+)	O TMDS		Passive level shifter shall use PD 470R.
TMDS_LANE0+ TMDS_LANE0-	143 145	TMDS differential pair lines lane 0. (Shared with DP_LANE2- and DP_LANE2+)	O TMDS		Passive level shifter shall use PD 470R.
TMDS_LANE1+ TMDS_LANE1-	137 139	TMDS differential pair lines lane 1. (Shared with DP_LANE1- and DP_LANE1+)	O TMDS		Passive level shifter shall use PD 470R.
TMDS_LANE2+ TMDS_LANE2-	149 151	TMDS differential pair lines lane 2. (Shared with DP_LANE0- and DP_LANE0+)	O TMDS		Passive level shifter shall use PD 470R.
HDMI_CTRL_CLK	152	DDC based control signal (clock) for TMDS device.	I/OD 3.3V	PU 2k2 3.3V	Level shifter FET and 2.2k PU to 5V shall be placed between module and TMDS connector.
HDMI_CTRL_DAT	150	DDC based control signal (data) for TMDS device.	I/OD 3.3V	PU 2k2 3.3V	Level shifter FET and 2.2k PU to 5V shall be placed between module and TMDS connector.
DP_HDMI_HPD#	153	Hot plug active low detection signal that serves as an interrupt request.	I 3.3V	PU 10k 3.3V	Supports open drain and PushPull Driver.

Note

The conga-QA5 does not natively support TMDS. A DP++ to TMDS converter (e.g. PTN3360D) needs to be implemented.

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Table 23 LPC Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
LPC_AD0 LPC_AD1 LPC_AD2 LPC_AD3	185 186 187 188	Multiplexed Command, Address and Data (LPC_AD[0..3])	I/O 3.3V	PU 20k	
LPC_FRAME#	190	LPC frame indicates the start of a new cycle or the termination of a broken cycle.	I/O 3.3V	PU 20k	
LPC_LDRQ#	192	LPC DMA request.	I 3.3V	PU 10k	Not supported.
LPC_CLK	189	LPC clock	O 3.3V		25 MHz.
SERIRQ	191	Serialized Interrupt.	I/O 3.3V	PU 20k	

Note

The conga-QA5 does not support GPIOs on the LPC interface.

Table 24 SPI Interface Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SPI_MOSI (**)	199	Master serial output/Slave serial input signal. SPI serial output data from Qseven® module to the SPI device.	O 3.3VSB		
SPI_MISO (**)	201	Master serial input/Slave serial output signal. SPI serial input data from the SPI device to Qseven® module.	I 3.3VSB		
SPI_SCK (**)	203	SPI clock output.	O 3.3VSB		
SPI_CS0# (**)	200	SPI chip select 0 output.	O 3.3VSB		
SPI_CS1#	202	SPI Chip Select 1 signal is used as the second chip select when two devices are used. Do not use when only one SPI device is used.	O 3.3VSB	PU 10k	Not supported

Note

The SPI interface is for external BIOS only.

On Intel Apollo Lake SoC, the signals marked with asterisks (**) have voltage levels that are different from the levels defined in the Qseven Specification. To comply with the Qseven Specification, the signals are routed through bidirectional level shifters on the module.

The bidirectional level shifters by nature have limited driving strength. congatec therefore recommends to route these signals as short as possible.

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Table 25 CAN Bus Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
CAN0_TX	129	CAN (Controller Area Network) TX output for CAN Bus channel 0. In order to connect a CAN controller device to the Qseven® module's CAN bus it is necessary to add transceiver hardware to the carrier board.	O 3.3V		Not connected
CAN0_RX	130	RX input for CAN Bus channel 0. In order to connect a CAN controller device to the Qseven® module's CAN bus it is necessary to add transceiver hardware to the carrier board.	I 3.3V		Not connected

Table 26 Power and GND Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
VCC	211-230	Power Supply +5VDC ±5%.	P		
VCC_5V_SB	205-206	Standby Power Supply +5VDC ±5%.	P		VCC_5V_SB should be connected to VCC if not used on carrier board.
VCC_RTC	193	3 V backup cell input. VCC_RTC should be connected to a 3V backup cell for RTC operation and storage register non-volatility in the absence of system power. (VCC_RTC = 2.5 - 3.3 V).	P		
GND	1, 2, 23-25, 34, 39-40, 57-58, 73-74, 97-98, 117-118, 135-136, 141-142, 147-148, 159-160, 165-166, 183-184, 197-198	Power Ground.	P		

Table 27 Power Control Signal Descriptions

Signal	Pin #	Description of Power Control signals	I/O	PU/PD	Comment
PWGIN	26	High active input for the Qseven® module indicates that all power rails located on the carrier board are ready for use.	I 5V	PU 10k 3.3V	Supports open drain and PushPull driver. The input is protected by diode on module.
PWRBTN#	20	Power Button: Low active power button input. This signal is triggered on the falling edge. **Note:** For proper detection, assert a pulse width of at least 16 ms.	I 3.3VSB	PU 10k 3.3VSB	

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Table 28 Power Management Signal Descriptions

Signal	Pin #	Description of Power Management signals	I/O	PU/PD	Comment
RSTBTN#	28	Reset button input. This input may be driven active low by an external circuitry to reset the Qseven® module. **Note:** For proper detection, assert a pulse width of at least 16 ms.	I 3.3V	PU 10k 3.3V	
BATLOW#	27	Battery low input. This signal may be driven active low by external circuitry to signal that the system battery is low or may be used to signal some other external battery management event.	I 3.3VSB	PU 10k 3.3VSB	
WAKE#	17	External system wake event. This may be driven active low by external circuitry to signal an external wake-up event.	I 3.3VSB	PU 10k 3.3VSB	
SUS_STAT#	19	Suspend Status: indicates that the system will be entering a low power state soon.	O 3.3VSB		
SUS_S3#	18	S3 State: This signal shuts off power to all runtime system components that are not maintained during S3 (Suspend to Ram), S4 or S5 states. The signal SUS_S3# is necessary in order to support the optional S3 cold power state.	O 3.3VSB		
SUS_S5#	16	S5 State: This signal indicates S4 or S5 (Soft Off) state.	O 3.3VSB		
SLP_BTN#	21	Sleep button. Low active signal used by the ACPI operating system to transition the system into sleep state or to wake it up again. This signal is triggered on falling edge. **Note:** For proper detection, assert a pulse width of at least 16 ms.	I 3.3VSB	PU 10k 3.3VSB	
LID_BTN#	22	LID button. Low active signal used by the ACPI operating system to detect a LID switch and to bring system into sleep state or to wake it up again. **Note:** For proper detection, assert a pulse width of at least 16 ms.	I 3.3VSB	PU 10k 3.3VSB	

Table 29 Miscellaneous Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
WDTRIG#	70	Watchdog trigger signal. This signal restarts the watchdog timer of the Qseven® module on the falling edge of a low active pulse.	I 3.3V	PU 10k 3.3V	
WDOUT	72	Watchdog event indicator. High active output used for signaling a missing watchdog trigger. Will be deasserted by software, system reset or a system power down.	O 3.3V		
GP0_I2C_CLK	66	Clock line of I²C bus.	I/OD 3.3V	PU 2k2 3.3V	
GP0_I2C_DAT	68	Data line of I²C bus.	I/OD 3.3V	PU 2k2 3.3V	
GP1_SMB_CLK	60	Clock line of System Management Bus.	I/OD 3.3VSB	PU 2k2 3.3VSB	
GP1_SMB_DAT	62	Data line of System Management Bus.	I/OD 3.3VSB	PU 2k2 3.3VSB	
SMB_ALERT#	64	System Management Bus Alert input. This signal may be driven low by SMB devices to signal an event on the SM Bus.	I/OD 3.3VSB	PU 10k 3.3VSB	
SPKR /GP_PWM_OUT2	194	Primary functionality is output for audio enunciator, the "speaker" in PC AT systems. When not in use for this primary purpose it can be used as General Purpose PWM Output.	O 3.3V		
BIOS_DISABLE# /BOOT_ALT#	41	Module BIOS disable input signal. Pull low to disable module's onboard BIOS. Allows off-module BIOS implementations. This signal can also be used to disable standard boot firmware flash device and enable an alternative boot firmware source, for example a bootloader.	I 3.3VSB	PU 10k 3.3VSB	
RSVD	132,134, 144, 146	Do not connect	NC		Not connected
GP_1-Wire_Bus	124	General Purpose 1-Wire bus interface.	I/O 3.3V		Not connected

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Table 30 Manufacturing Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
MFG_NC0	207	This pin is reserved for manufacturing and debugging purposes. May be used as JTAG_TCK signal for boundary scan purposes during production or as a vendor specific control signal. When used as a vendor specific control signal the multiplexer must be controlled by the MFG_NC4 signal.	NA	NA	
MFG_NC1	209	This pin is reserved for manufacturing and debugging purposes. May be used as JTAG_TDO signal for boundary scan purposes during production. May also be used, via a multiplexer, as a UART_TX signal to connect a simple UART for firmware and boot loader implementations. In this case the multiplexer must be controlled by the MFG_NC4 signal.	NA	NA	
MFG_NC2	208	This pin is reserved for manufacturing and debugging purposes. May be used as JTAG_TDI signal for boundary scan purposes during production. May also be used, via a multiplexer, as a UART_RX signal to connect a simple UART for firmware and boot loader implementations. In this case the multiplexer must be controlled by the MFG_NC4 signal.	NA	NA	
MFG_NC3	210	This pin is reserved for manufacturing and debugging purposes. May be used as JTAG_TMS signal for boundary scan purposes during production. May also be used, via a multiplexer, as vendor specific BOOT signal for firmware and boot loader implementations. In this case the multiplexer must be controlled by the MFG_NC4 signal.	NA	NA	
MFG_NC4	204	This pin is reserved for manufacturing and debugging purposes. May be used as JTAG_TRST# signal for boundary scan purposes during production. May also be used as control signal for a multiplexer circuit on the module enabling secondary function for MFG_NC0..3 (JTAG / UART). When MFG_NC4 is high active it is being used for JTAG purposes. When MFG_NC4 is low active it is being used for UART purposes.	NA	NA	

Note

The carrier board must not drive the MFG_NC-pins or have pull-up or pull-down resistors implemented for these signals.

Table 31 Thermal Management Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
THRM#	69	Thermal Alarm active low signal generated by the external hardware to indicate an over temperature situation. This signal can be used to initiate thermal throttling.	I 3.3V	PU 10k 3.3V	
THRMTRIP#	71	Thermal Trip indicates an overheating condition of the processor. If 'THRMTRIP#' goes active the system immediately transitions to the S5 State (Soft Off).	O 3.3V		

Table 32 Fan Control Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
FAN_PWMOUT	196	Primary functionality is fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the Fan's RPM based on the CPU's die temperature. .	O 3.3V	PU 10k 3.3V	
FAN_TACHOIN	195	Primary functionality is fan tachometer input.	I 3.3V	PU 10k 3.3V	

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9 System Resources

9.1 I/O Address Assignment

The I/O address assignment of the conga-QA5 module is functionally identical with a standard PC/AT.

Table 33 I/O Address Assignment

I/O Address (hex)	Size	Available	Description
0000h - 00FFh	256 bytes	No	Motherboard resources
03B0h - 03CFh	32 bytes	No	Video system
400h - 47Fh	128 bytes	No	Motherboard resources
500h - 5FFh	256 bytes	No	Motherboard resources
680h - 69Fh	20 bytes	No	Motherboard resources
0CF8h - 0CFBh	4 bytes	No	PCI configuration address register
0CFCh - 0CFFh	4 bytes	No	PCI configuration data register
0D00h - F000h		See note	PCI / PCI Express bus

Note

The BIOS assigns PCI and PCI Express I/O resources from F000h downwards. Devices, which are not PnP/PCI/PCI Express compliant, must not use I/O resources in that area.

9.1.1 LPC Bus

On the conga-QA5, the internal PCI Bus acts as the substractive decoding agent. All I/O cycles that are not positively decoded are forwarded to the PCI Bus, not the LPC Bus. Only specified I/O ranges are forwarded to the LPC Bus. With the default settings in the congatec Embedded BIOS, the following I/O address ranges are sent to the LPC Bus:

80h - 8Fh via LPC Generic I/O Range 1
A00h - A1Fh via LPC Generic I/O Range 4

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The following I/O decode ranges are fixed to the LPC Bus:

2Eh - 2Fh
4Eh - 4Fh
200h - 20Fh
2F8h - 2FFh
3F8h - 3FFh
378h - 37Fh
778h - 77Fh
3F0h - 3F5h
3F7h, 60h, 62h, 64h, 66h

Parts of these ranges are not available if Super I/O is used on the carrier board. If Super I/O is not implemented on the carrier board, then all these ranges are available for customer use. If you require additional LPC Bus resources other than those mentioned above, or more information about this subject, contact congatec technical support for assistance.

9.2 PCI Configuration Space Map

Table 34 PCI Configuration Space Map

Bus Number (hex)	Device Number (hex)	Function Number (hex)	Device ID	Description and Device ID
00h	00h	00h	0x5AF0	Host Bridge
00h	02h	00h	0x5A84	Graphics and Display
00h	0Dh	00h	0x5A92	Primary to SideBand Bridge
00h	0Dh	01h	0x5A94	PMC (Power Management Controller)
00h	0Dh	02h	0x5A96	Fast SPI
00h	0Dh	03h	0x5AEC	Shared SRAM
00h	0Eh	00h	0x5A98	HDA
00h	0Fh	00h	0x5A9A	Simple Communication Controller 0
00h	0Fh	01h	0x5A9C	Simple Communication Controller 1
00h	0Fh	02h	0x5A9E	Simple Communication Controller 2
00h	012h	00h	0x5AE3	SATA
00h	013h	00h	0x5AD8	PCIe -A0 *1
00h	013h	01h	0x5AD9	PCIe -A1 *1
00h	013h	02h	0x5ADA	PCIe -A2 *1
00h	013h	03h	0x5ADB	PCIe -A3 *1
00h	014h	00h	0x5AD6	PCIe -B0
00h	015h	00h	0x5AA8	USB-Host (xHCI)
00h	015h	01h	0x5AAA	USB-Host (xDCI)
00h	016h	00h	0x5AAC	I2C 0 *2

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00h	016h	01h	0x5AAE	I2C 1 *2
00h	016h	02h	0x5AB0	I2C 2 *2
00h	016h	03h	0x5AB2	I2C 3 *2
00h	017h	00h	0x5AB4	I2C 4 *2
00h	017h	00h	0x5AB6	I2C 5 *2
00h	017h	00h	0x5AB8	I2C 6 *2
00h	017h	00h	0x5ABA	I2C 7 *2
00h	018h	00h	0x5ABC	SoC UART 0 *2
00h	018h	01h	0x5ABE	SoC UART 1 *2
00h	018h	02h	0x5AC0	SoC UART 2 *2
00h	018h	03h	0x5AEE	SoC UART 3 *2
00h	019h	00h	0x5AC2	SPI 0 *2
00h	019h	01h	0x5AC4	SPI 1 *2
00h	019h	02h	0x5AC6	SPI 2 *2
00h	01Bh	00h	0x5ACA	SD Card
00h	01Ch	01h	0x5ACC	eMMC
00h	01Fh	00h	0x5AE8	LPC Bus
00h	01Fh	01h	0x5AD4	SM Bus
02h	00h	00h	0x1539	Intel PCIe Ethernet Network on Module

Note

The above table represents a case when a single function PCI Express device is connected to all possible slots on the carrier board. The given bus numbers will change based on actual hardware configuration.

**1 The PCI Express Ports may only be visible if the PCI Express Port is set to "Enabled" in the BIOS setup program and a device is attached to the corresponding PCI Express port on the carrier board.*

**2 This device is disabled as default in BIOS Setup.*

9.3 I²C Bus

There are no onboard resources connected to the I²C bus. Address 16h is reserved for congatec Battery Management solutions.

9.4 SM Bus

System Management (SM) bus signals are connected to the Intel Apollo Lake SoC and the SM bus is not intended to be used by off-board non-system management devices. For more information about this subject contact congatec technical support.

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9.5 congatec System Sensors

conga-QA5 offers several sensors and monitors accessible through CGOS interface and also visible on the Health Monitor Submenu in BIOS Setup:

- Two temperature sensors
  - CPU temperature based on CPU digital thermal sensor
  - Board temperature sensor located on the board controller
- Two voltage sensors
  - 5V standard voltage sensor
  - 5V standby voltage sensor
- One current Sensor
- One fan monitor

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10 BIOS Setup Description

The BIOS setup description of the conga-QA5 can be viewed without having access to the module. However, access to the restricted area of the congatec website is required in order to download the necessary tool (CgMlfViewer) and Menu Layout File (MLF).

The MLF contains the BIOS setup description of a particular BIOS revision. The MLF can be viewed with the CgMlfViewer tool. This tool offers a search function to quickly check for supported BIOS features. It also shows where each feature can be found in the BIOS setup menu.

For more information, read the application note "AN42 - BIOS Setup Description" available at www.congatec.com.

Note

If you do not have access to the restricted area of the congatec website, contact your local congatec sales representative.

10.1 Navigating the BIOS Setup Menu

The BIOS setup menu shows the features and options supported in the congatec BIOS. To access and navigate the BIOS setup menu, press the <DEL> or <F2> key during POST.

The right frame displays the key legend. Above the key legend is an area reserved for text messages. These text messages explain the options and the possible impacts when changing the selected option in the left frame.

10.2 BIOS Versions

The BIOS displays the BIOS project name and the revision code during POST, and on the main setup screen. The initial production BIOS for conga-QA5 is identified as QA50R1xx, where:

- QA50 is the project name
- R is the identifier for a BIOS ROM file
- 1 is the feature number
- xx is the major and minor revision number.

The binary size of conga-QA5 BIOS is 8 MB.

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10.3 Updating the BIOS

BIOS updates are recommended to correct platform issues or enhance the feature set of the module. The conga-QA5 features a congatec/AMI AptioEFI firmware on an onboard flash ROM chip. You can update the firmware with the congatec System Utility. The utility has five versions—UEFI shell, DOS based command line[1], Win32 command line, Win32 GUI, and Linux version.

For more information about "Updating the BIOS" refer to the user's guide for the congatec System Utility "CGUTLm1x.pdf" on the congatec website at www.congatec.com.

Note

1. *Deprecated*

Caution

The DOS command line tool is not officially supported by congatec and therefore not recommended for critical tasks such as firmware updates. We recommend to use only the UEFI shell for critical updates.

10.4 Supported Flash Devices

The conga-QA5 supports the following flash device:

- Winbond W25Q64JVSSIQ (8 MB)

The flash device listed above can be used on the carrier board for external BIOS support. For more information about external BIOS support, refer to the Application Note "AN7_External_BIOS_Update.pdf" on the congatec website at www.congatec.com.

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