SMARC® conga-SA5

SMARC 2.1 module based on the Intel® Atom®, Pentium® and Celeron® Apollo Lake SoC

User's Guide

Revision 1.11

Revision History

Revision	Date (yyyy-mm-dd)	Author	Changes
0.1	2017-08-16	AEM	• Preliminary release
1.0	2017-10-20	AEM	• Updated TPM support in tables 1 and 2 of section 1.2.1 "Options Information • Added TPM support to table 3 "Feature Summary" • Removed Android from supported OS in section 2.2 "Supported Operating Systems" • Updated table 5 "Power Consumptions Values" and table 6 "CMOS Battery Power Consumption" • Updated table 28 "GPIO Signal Description" • Added content to section 9 "System Resources" and section 10 "BIOS Setup Description" • Official release
1.1	2018-05-02	AEM	• Updated "Electrostatic Sensitive Device" information on page 3 • Corrected the power consumption measurement unit in table 5 "Power Consumption Values" • Corrected the number of supported PCIe gen 2 lanes in section 1.2.1 "Options Information" • Corrected the onboard memory capacity of the variant with PN: 050010 in table 2 "conga-SA5 (Industrial Variants) • Added section 2.4.3 "Rise Time" • Corrected typographical error in table 30.1 "Boot Source Description" • Added EFT caution to section 5.5 "Universal Serial Bus (USB)" • Updated section 5.8 "UART" • Corrected the signal name of pin 37 in table 16 "SDIO Signal Descriptions" • Corrected the list of supported flash devices in section 10.4 "Supported Flash Devices"
1.2	2018-06-25	AEM	• Added errata as a document to read in the preface section • Corrected the description of HDMI_HPD signal in table 14 "HDMI Signal Descriptions" • Updated tables 11 "SMARC Edge Finger Pinout" and 18 "eSPI/SPI1 Signal Descriptions"
1.3	2018-08-21	AEM	• Corrected the power consumption of Intel® Pentium N4200 at peak value in table 5 "Power Consumption Values"
1.4	2018-10-29	AEM	• Updated section 4 "Cooling Solutions" to reflect the new height of the fins • Added note about PCIe reference clocks in section 5.2 "PCIe Express™" • Added note about UART legacy mode in section 5.8 "UART" • Corrected the Winbond flash supported for external BIOS in section 10.4 "Supported Flash Devices"
1.5	2019-06-06	AEM	• Updated the product image on the title page • Added Intel® Celeron® J3455 variant to table 1 and 5 • Updated the website link for SMARC specification and design guide • Added table 9"PCIe Reference Clock Configuration" • Updated table 30 "GPIO Signal Description"
1.6	2019-09-20	AEM	• Corrected the number of available variants in section 1.2.1 "Options Information" • Added variants with part numbers 050003 and 050013 to table 1" Commercial Variants", and variant with part number 050031 to table 2 "Industrial Variants" • Updated the recommended maximum torque for cooling solutions in section 4 "Cooling Solutions" • Combined section 5.11 "I2S" and section 5.7 "Audio (HDA/I2S)". Also added note about I2S driver for Windows OS • Updated section 6 "Additional Features". Also added section 6.2 "Security Features" • Deleted section 6.2.1.6 "I²C Bus" • Updated section 10.3 "Updating the BIOS"

1.7	2020-04-06	AEM	• Updated section 5.2 "PCI Express" and added section 5.2.2 "PCIe Link Configuration" • Added SPI TPM support to section 5.10 "SPI" • Corrected the discrete TPM bus in section 6.2 "Security Features" • Corrected signal names of pins S5 and S7 in table 13 "SMARC Edge Finger Pinout" as indicated in SMARC_V2_errata1.1.pdf document • Updated the link for the power supply design guide in section 5.1.2 "Power Control" • Added chip select information for SPI TPM to table 19 "SPI0 Signal Descriptions" • Added note about the minimum pulse width required for proper button detection in table 31 "Management Pins Signal Description" • Updated section 10 "BIOS Setup Description" • Delected section 11 "Industrial Specifications"
1.8	2020-07-03	AEM	• Rephrased the note about boot source configuration in table 32.1 "Boot Source Description" • Added note that custom BIOS is required for SPI TPM support in section5.10 "SPI" and table 19 "SPI0 Signal Descriptions"
1.9	2020-12-01	AEM	• Deleted I2S support from section 5.7 "Audio (HDA/I2S) • Deleted I2S signals from table 22 "HDA/I2S Signal Descriptions" • Updated the note in section 5.8 "UART" • Updated the comment in table 24 "Asynchronous Serial Port Signal Description" • Removed I2S0_SDOUT signal from table 32.2 "Boot strap Signal Descriptions"
1.10	2021-07-31	AEM	• Added Software License Information • Changed congatec AG to congatec GmbH • Corrected the storage temperature for industrial variants in section 2.7 "Environmental Specifications" • Updated Power Supply Implementation Guidelines in section 5.12 "Power Control" • Updated section 6.6 "congatec Battery Management Interface" • Added note about HDMI operation to table 15 "HDMI Signal Descriptions" • Moved section 9.4 "congatec System Sensors" to section 6.8
1.11	2021-11-08	AEM	• Corrected the SMARC revision from 2.0 to 2.1

Preface

This user's guide provides information about the components, features, connectors and BIOS Setup menus available on the conga-SA5. It is one of four documents that should be referred to when designing a SMARC® application. This user's guide should be read in conjunction with the document "Errata_congatec_xA5_designs". Click on the document name to download it.

The other reference documents that should be used include the following:

SMARC® Design Guide 2.0
SMARC® Specification 2.1

The links to the SMARC® documents can be found on the SGET website at www.sget.org.

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Terminology

Term	Description
GB	Gigabyte
GHz	Gigahertz
kB	Kilobyte
MB	Megabyte
MTps	Mega-transfers per second
Mbit	Megabit
kHz	Kilohertz
MHz	Megahertz
TDP	Thermal Design Power
cBC	congatec Board Controller
PCIe	PCI Express
SATA	Serial ATA
PEG	PCI Express Graphics
PCH	Platform Controller Hub
eDP	Embedded DisplayPort
DDI	Digital Display Interface
HDA	High Definition Audio
N.C	Not connected
N.A	Not available
T.B.D	To be determined

Contents

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1 Introduction

1.1 SMARC® Concept

The Standardization Group for Embedded Technologies e.V (SGET) defined the SMARC standard for small form factor computer modules that target applications with ultra low power, low cost and high performance. The SMARC connector and interfaces are optimized for high-speed communication, and are suitable for ARM SoCs and low power x86 SoCs.

The SMARC standard bridges the gap between the COM Express standard and the Qseven standard by offering most of the interfaces defined in the COM Express specification at a lower power. With a footprint of 82 mm x 50 mm or 82 mm x 80 mm, the SMARC standard promotes the design of highly integrated, energy efficient systems.

Due to its small size and lower power demands, PC appliance designers can design low cost devices as well as explore a huge variety of product development options—from compact space-saving designs to fully functional systems. This solution allows scalability, product diversification and faster time to market.

1.2 conga-SA5 Options Information

The conga-SA5 is designed based on the SMARC 2.1 Specification. The conga-SA5 features the Intel® Atom, Pentium and Celeron Apollo Lake SoCs. With maximum 12 W TDP, the conga-SA5 offers Ultra Low Power boards with high computing performance and outstanding graphics. Additionally, the conga-SA5 supports quad channel LPDDR4 memory with up 8 GB capacity and data rates up to 2400 MTps, multiple I/O interfaces, up to three independent displays and various congatec embedded features.

By offering most of the functional requirement for any SMARC application, the conga-SA5 provides manufacturers and developers with a platform to jump-start the development of systems and applications based on SMARC specification. Its features and capabilities make it an ideal platform for designing compact, energy-efficient, performance-oriented embedded systems.

1.2.1 Options Information

The conga-SA5 is available in 12 variants (eight commercial and four industrial). The tables below show the different configurations available.

Table 1 Commercial Variants

Part-No		050000	050001	050002	050003	050022
Processor		Intel® Atom® x7-E3950, 1.6 GHz, Quad Core	Intel® Atom® x5-E3940, 1.6 GHz, Quad Core	Intel® Atom® x5-E3930, 1.3 GHz, Dual Core	Intel® Atom® x5-E3930, 1.3 GHz, Dual Core	Intel® Celeron® N3350, 1.1 GHz, Dual Core
Burst Freq.		2.0 GHz	1.8 GHz	1.8 GHz	1.8 GHz	2.4 GHz
L2 Cache		2 MB	2 MB	2 MB	2 MB	2 MB
Graphics Engine		Intel® HD Graphics 505	Intel® HD Graphics 500	Intel® HD Graphics 500	Intel® HD Graphics 500	Intel® HD Graphics 500
GFX Base/Burst Freq.		500 / 650 MHz	400 / 600 MHz	400 / 550 MHz	400 / 550 MHz	200 / 650
Onboard Memory (LPDDR4)		8 GB, 2400 MTps quad channel	4 GB, 2133 MTps quad channel	2 GB, 2133 MTps dual channel	2 GB, 2133 MTps dual channel	4 GB, 2400 MTps quad channel
PCIe		4x Gen2	4x Gen2	4x Gen2	4x Gen2	4x Gen2
Ethernet		2x i211	2x i211	2x i211	1x i211	2x i211
Display Interfaces	LVDS	Single/Dual 18/24 bit	Single/Dual 18/24 bit	Single/Dual 18/24 bit	Single/Dual 18/24 bit	Single/Dual 18/24 bit
	DP++	1x DP++	1x DP++	1x DP++	1x DP++	1x DP++
	HDMI	1x native HDMI	1x native HDMI	1x native HDMI	1x native HDMI	1x native HDMI
USB ports		4x USB 2.0 2x USB 3.0/2.0	4x USB 2.0 2x USB 3.0/2.0	4x USB 2.0 2x USB 3.0/2.0	4x USB 2.0 2x USB 3.0/2.0	4x USB 2.0 2x USB 3.0/2.0
eMMC		32 GB	32 GB	16 GB	16 GB	32 GB
Wifi/BT Module		N.A	N.A	N.A	N.A	N.A
TPM	Firmware	Intel® PTT	Intel® PTT	Intel® PTT	Intel® PTT	Intel® PTT
	Discrete	N.A	N.A	N.A	N.A	N.A
SD Card		1x 4-bit	1x 4-bit	1x 4-bit	1x 4-bit	1x 4-bit
Max. TDP		12 W	9.5 W	6.5 W	6.5 W	6 W

Part-No		050023	050024	050031
Processor		Intel® Pentium® N4200, 1.1 GHz, Quad Core	Intel® Celeron® J3455, 1.5 GHz, Quad Core	Intel® Atom® x7-E3950, 1.6 GHz, Quad Core
Burst Freq.		2.5 GHz	2.3 GHz	2.0 GHz
L2 Cache		2 MB	2 MB	2 MB
Graphics Engine		Intel® HD Graphics 505	Intel® HD Graphics 500	Intel® HD Graphics 505
GFX Base/Burst Freq.		200 / 750	250 / 750	500 / 650 MHz
Onboard Memory (LPDDR4)		8 GB, 2400 MTps quad channel	4 GB, 2400 MTps quad channel	8 GB, 2400 MTps quad channel
PCIe		4x Gen2	4x Gen2	4x Gen2
Ethernet		2x i211	2x i211	2x i211
Display Interfaces	LVDS	Single/Dual 18/24 bit	Single/Dual 18/24 bit	Single/Dual 18/24 bit
	DP++	1x DP++	1x DP++	1x DP++
	HDMI	1x native HDMI	1x native HDMI	1x native HDMI
USB ports		4x USB 2.0 2x USB 3.0/2.0	4x USB 2.0 2x USB 3.0/2.0	4x USB 2.0 2x USB 3.0/2.0
eMMC		32 GB	16 GB	32 GB
Wifi/BT Module		N.A	N.A	Sparklan WNSQ-261ACN
TPM	Firmware	Intel® PTT	Intel® PTT	Intel® PTT
	Discrete	N.A	N.A	Infineon SLB96665
SD Card		1x 4-bit	1x 4-bit	1x 4-bit
Max. TDP		6 W	10 W	12 W

Table 2 Industrial Variants

Part-No		050010	050011	050012	050013
Processor		Intel® Atom® x7-E3950, 1.6 GHz, Quad Core	Intel® Atom® x5-E3940, 1.6 GHz, Quad Core	Intel® Atom® x5-E3930, 1.3 GHz, Dual Core	Intel® Atom® x7-E3950, 1.6 GHz, Quad Core
Burst Freq.		2.0 GHz	1.8 GHz	1.8 GHz	2.0 GHz
L2 Cache		2 MB	2 MB	1 MB	2 MB
Graphics Engine		Intel® HD Graphics 505	Intel® HD Graphics 500	Intel® HD Graphics 500	Intel® HD Graphics 505
GFX Base/Burst Freq.		500 / 650 MHz	400 / 600 MHz	400 / 550 MHz	500 / 650 MHz
Onboard Memory (LPDDR4)		4 GB, 2400 MTps quad channel	4 GB, 2133 MTps quad channel	2 GB 2133 MTps dual channel	8 GB, 2400 MTps quad channel
PCIe		4x Gen2	4x Gen2	4x Gen2	4x Gen2
Ethernet		2x i210	2x i210	2x i210	2x i210
Display Interfaces	LVDS	Single/Dual 18/24 bit	Single/Dual 18/24 bit	Single/Dual 18/24 bit	Single/Dual 18/24 bit
	DP++	1x DP++	1x DP++	1x DP++	1x DP++
	HDMI	1x native HDMI	1x native HDMI	1x native HDMI	1x native HDMI
USB ports		4x USB 2.0 2x USB 3.0/2.0	4x USB 2.0 2x USB 3.0/2.0	4x USB 2.0 2x USB 3.0/2.0	4x USB 2.0 2x USB 3.0/2.0
eMMC		32 GB	32 GB	16 GB	32 GB
Wifi/BT Module		Optional	Optional	Optional	Optional
TPM	Firmware	Intel® PTT	Intel® PTT	Intel® PTT	Intel® PTT
	Discrete	N.A	N.A	N.A	N.A
SD Card		1x 4-bit	1x 4-bit	1x 4-bit	1x 4-bit
Max. TDP		12 W	9.5 W	6.5 W	12 W

2 Specifications

2.1 Feature List

Table 3 Feature Summary

Form Factor	SMARC® form factor specification, revision 2.1 (82 mm x 50 mm)
SoC	Intel® Atom®, Pentium® and Celeron SoCs
Memory	Onboard non-ECC LPDDR4 memory. Supports - Data rates up to 2400 MTps - Up to 8 GB capacity
congatec Board Controller	Multi-stage watchdog, non-volatile user data storage, manufacturing and board information, board statistics, hardware monitoring, fan control, I2C bus, Power loss control
Chipset	Integrated in the SoC
Audio	High Definition Audio interface with support for multiple codecs
Ethernet	2x Gigabit Ethernet via Intel® i210 and i211 controllers
Graphics Options	Next Generation Intel® HD (500/505). Supports: - API (DirectX 12, OpenGL 4.3, OpenCL 2.0, OpenGL ES 3.0) - Intel® QuickSync & Clear Video Technology HD (hardware accelerated video decode/encode/processing/transcode) - Up to 3 independent displays (must be two DDI's and one eDP/DSI/LVDS)
	1x LVDS (dual channel) 1x DP++ (DDI0) 1x HDMI (native) 2x MIPI-CSI (x4 and x2 lanes) **Optional Interface (assembly option)**: - 1x eDP 1.4 [1] - 1x DSI [2] - 1x DP++ (DDI1) [3] **NOTE**: 1 *LVDS is not supported with this option* 2 *Dual LVDS channel is not supported with this option* 3 *Native HDMI is not supported with this option*
Peripheral Interfaces	1x SATA® 6 Gbps Up to 4x PCIe® Gen2 ports USB Interfaces - 4x USB 2.0 - 2x USB 3.0/2.0 4x UART (two with handshake signals) 1x SD/SDIO eMMC 5.0 (up to 64 GB) Buses - 2x I²C - up to 2x I²S - 2x SPI (eSPI and SPI) **Optional Interface (assembly option)**: - M.2 1216 Wi-fi module - Discrete TPM 2.0
BIOS	AMI Aptio® V UEFI 2.x firmware, 8 MB serial SPI with congatec Embedded BIOS features
Power Mgmt.	ACPI 5.0 compliant with battery support. Also supports Suspend to RAM (S3)

Security	Firmware TPM 2.0 (Intel® PTT) Discrete LPC TPM 2.0 (Infineon SLB9665) or LPC TPM 1.2 (Infineon SLB9660) support via assembly option

Note

Some of the features above are optional.

2.2 Supported Operating Systems

The conga-SA5 supports the following operating systems.

- Microsoft® Windows® 10 IoT Enterprise
- Microsoft® Windows® IoT Core
- Microsoft® Windows® 10
- Linux 3.x / 4.x
- Yocto 2.x

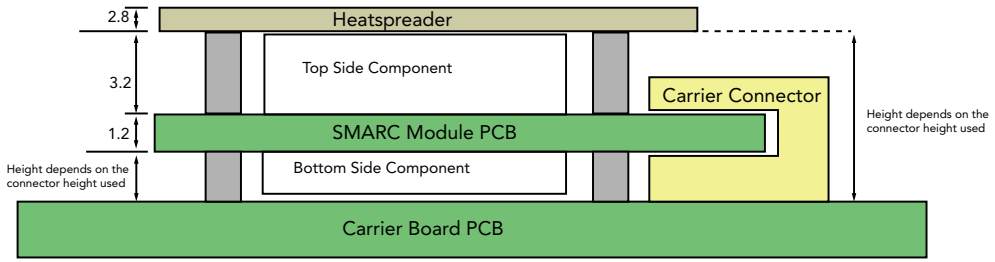
Note

Windows® 10 installation requires a minimum storage capacity of 20 GB. We will not offer installation support for systems with less than 20 GB storage space.

2.3 Mechanical Dimensions

- 82.0 mm x 50.0 mm

The height of the module, the heatspreader and the stack is shown below:

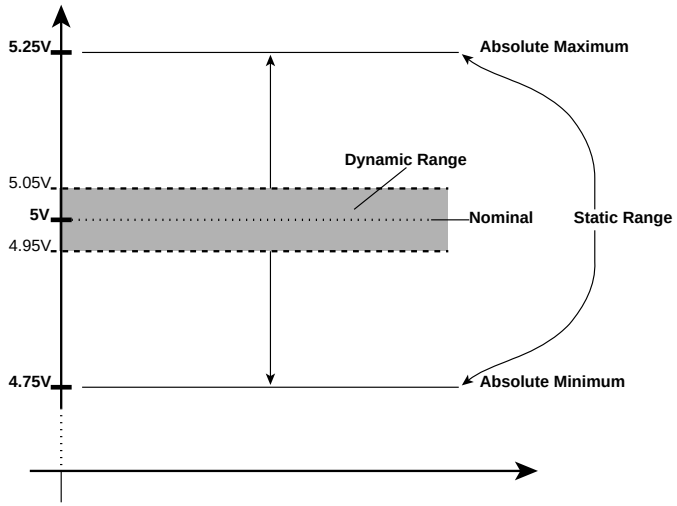


All dimensions are in millimeters

2.4 Standard Power

2.4.1 Supply Voltage

- 4.75 V – 5.25 V



2.4.2 Electrical Characteristics

Characteristics			Min.	Typ.	Max.	Units	Comment
5 V	Voltage	± 5%	4.75	5.00	5.25	Vdc	
	Ripple		-	-	± 50	mV_{PP}	0-20MHz
	Current						

2.4.3 Rise Time

The input voltages shall rise from 10 percent of nominal to 90 percent of nominal at a minimum slope of 250 V/s. The smooth turn-on requires that, during the 10 percent to 90 percent portion of the rise time, the slope of the turn-on waveform must be positive.

2.5 Power Consumption

The power consumption values were measured with the following setup:

- Input voltage +5 V
- conga-SA5 COM
- conga-SEVA carrier board
- conga-SA5 cooling solution
- Microsoft Windows 10 (64 bit)

Table 4 Measurement Description

The power consumption values were recorded during the following system states:

System State	Description	Comment
S0: Minimum value	Lowest frequency mode (LFM) with minimum core voltage during desktop idle	
S0: Maximum value	Highest frequency mode (HFM/Turbo Boost)	The CPU was stressed to its maximum frequency
S0: Peak value	Highest power spike during the measurement of "S0: Maximum value". This state shows the peak value over a short period of time (worst case power consumption value)	Consider this value when designing the system's power supply to ensure that sufficient power is supplied during worst case scenarios
S3	COM is powered by VCC_5V, while in Suspend to RAM state	
S5	COM is powered by VCC_5V, while in Soft-Off state	

Note

The peripherals did not influence the measured values because they were powered externally.

Table 5 Power Consumption Values

The table below provides additional information about the conga-SA5 power consumption. The values are recorded at various operating mode.

Part No.	Memory Size	H.W Rev.	BIOS Rev.	OS (64 bit)	CPU			Current (A)				
					Variant	Cores	Freq. /Max. Turbo	S0: Min	S0: Max	S0: Peak	S3	S5
050000	8 GB	A.0	R019	Windows 10	Intel® Atom® x7-E3950	4	1.6 / 2.0 GHz	0.37	3.90	4.22	0.12	0.12
050001	4 GB	A.0	R019	Windows 10	Intel® Atom® x7-E3940	4	1.6 / 1.8 GHz	0.40	3.12	4.22	0.10	0.07
050002	2 GB	A.0	R019	Windows 10	Intel® Atom® x7-E3930	2	1.3 / 1.8 GHz	0.39	2.28	2.49	0.10	0.10
050010	8 GB	A.0	R019	Windows 10	Intel® Atom® x7-E3950	4	1.6 / 2.0 GHz	0.37	3.90	4.22	0.12	0.12
050011	4 GB	A.0	R019	Windows 10	Intel® Atom® x7-E3940	4	1.6 / 1.8 GHz	0.40	3.12	4.22	0.10	0.07
050012	2 GB	A.0	R019	Windows 10	Intel® Atom® x7-E3930	2	1.3 / 1.8 GHz	0.39	2.28	2.49	0.10	0.10
050022	4 GB	A.0	R019	Windows 10	Intel® Celeron® N3350	2	1.1 / 2.3 GHz	0.39	2.41	4.17	0.13	0.10
050023	8 GB	A.0	R019	Windows 10	Intel® Pentium® N4200	4	1.1 / 2.5 GHz	0.39	2.46	4.26	0.14	0.11
050024	4 GB	B.0	R137	Windows 10	Intel® Celeron® J3455	4	1.5 / 2.3 GHz	0.45	3.08	5.44	0.08	0.07

2.6 Supply Voltage Battery Power

Table 6 CMOS Battery Power Consumption

RTC @	Voltage	Current
-10°C	3V DC	1.48 µA
20°C	3V DC	1.63 µA
70°C	3V DC	2.72 µA

Note

1. *Do not use the CMOS battery power consumption values listed above to calculate CMOS battery lifetime.*
2. *Measure the CMOS battery power consumption in your customer specific application in worst case conditions (for example, during high temperature and high battery voltage).*
3. *Consider the self-discharge of the battery when calculating the lifetime of the CMOS battery. For more information, refer to application note AN9_RTC_Battery_Lifetime.pdf on congatec GmbH website at www.congatec.com/support/application-notes.*
4. *We recommend to always have a CMOS battery present when operating the conga-SA5*

2.7 Environmental Specifications

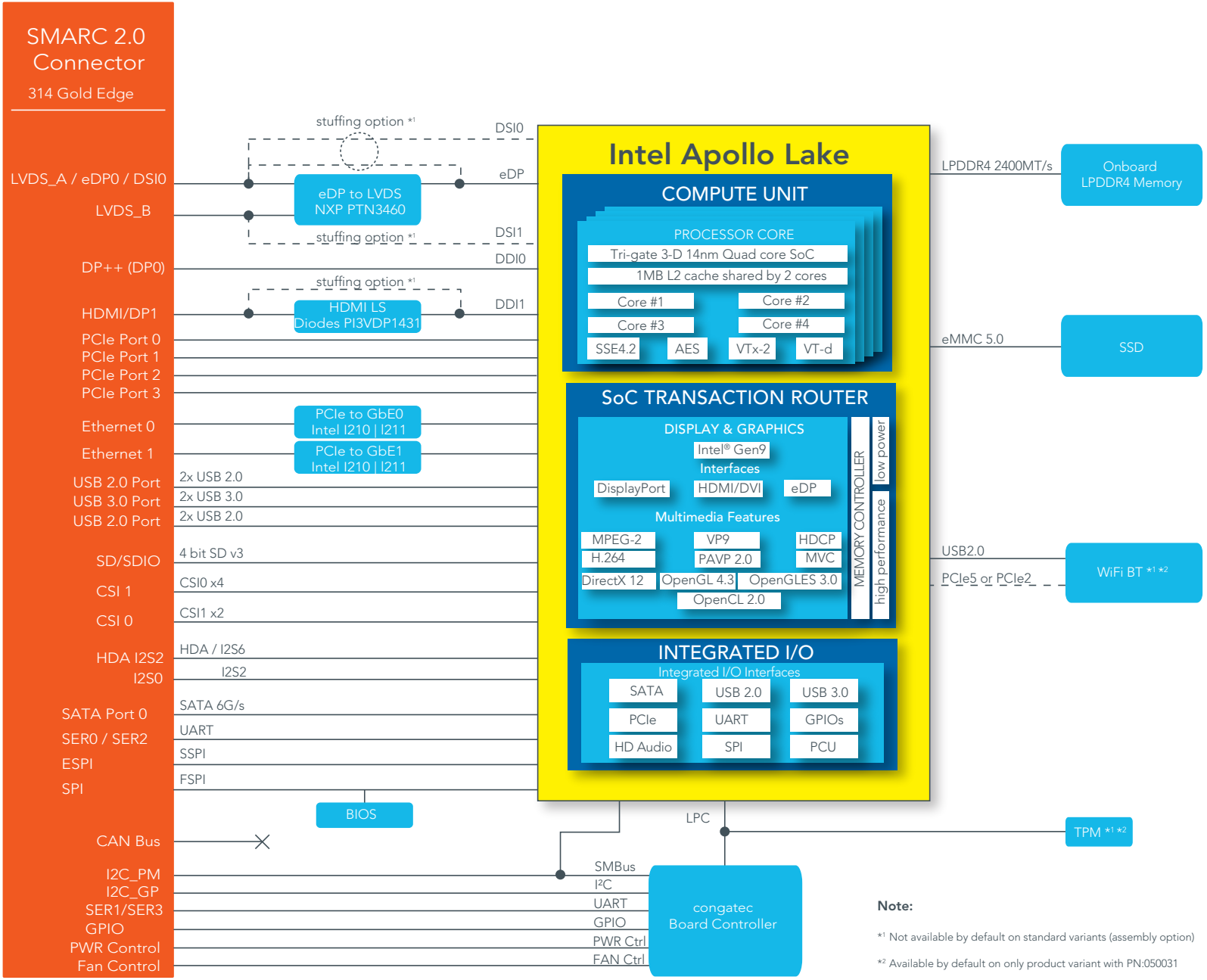
Temperature (commercial variants)	Operation: 0° to 60°C	Storage: -20° to +80°C
Temperature (industrial variants)	Operation: -40° to 85°C	Storage: -40° to +85°C
Humidity	Operation: 10% to 90%	Storage: 5% to 95%

Caution

The above operating temperatures must be strictly adhered to at all times. When using a congatec heatspreader, the maximum operating temperature refers to any measurable spot on the heatspreader's surface.

Humidity specifications are for non-condensing conditions.

3 Block Diagram



4 Cooling Solutions

congatec GmbH offers the following cooling solutions for the conga-SA5. The dimensions of the cooling solutions are shown in the sub-sections. All measurements are in millimeters.

Table 7 Cooling Solution Variants

	Cooling Solution	Part No	Description
1	CSP	050051	Passive cooling with 2.7 mm bore-hole standoffs for lidded CPU variants
		050055	Passive cooling with 2.7 mm bore-hole standoffs for bare-die CPU variants
2	HSP	050053	Heatspreader with 2.7 mm bore-hole standoffs for lidded CPU variants
		050057	Heatspreader with 2.7 mm bore-hole standoffs for bare-die CPU variants
3	CSA Adapter	050060	CSA adapter for passive coolers and heatspreaders

Note

1. *We recommend a maximum torque of 0.4 Nm for carrier board mounting screws and 0.5 Nm for module mounting screws.*

2. *The gap pad material used on congatec heatspreaders may contain silicon oil that can seep out over time depending on the environmental conditions it is subjected to. For more information about this subject, contact your local congatec sales representative and request the gap pad material manufacturer's specification.*

Caution

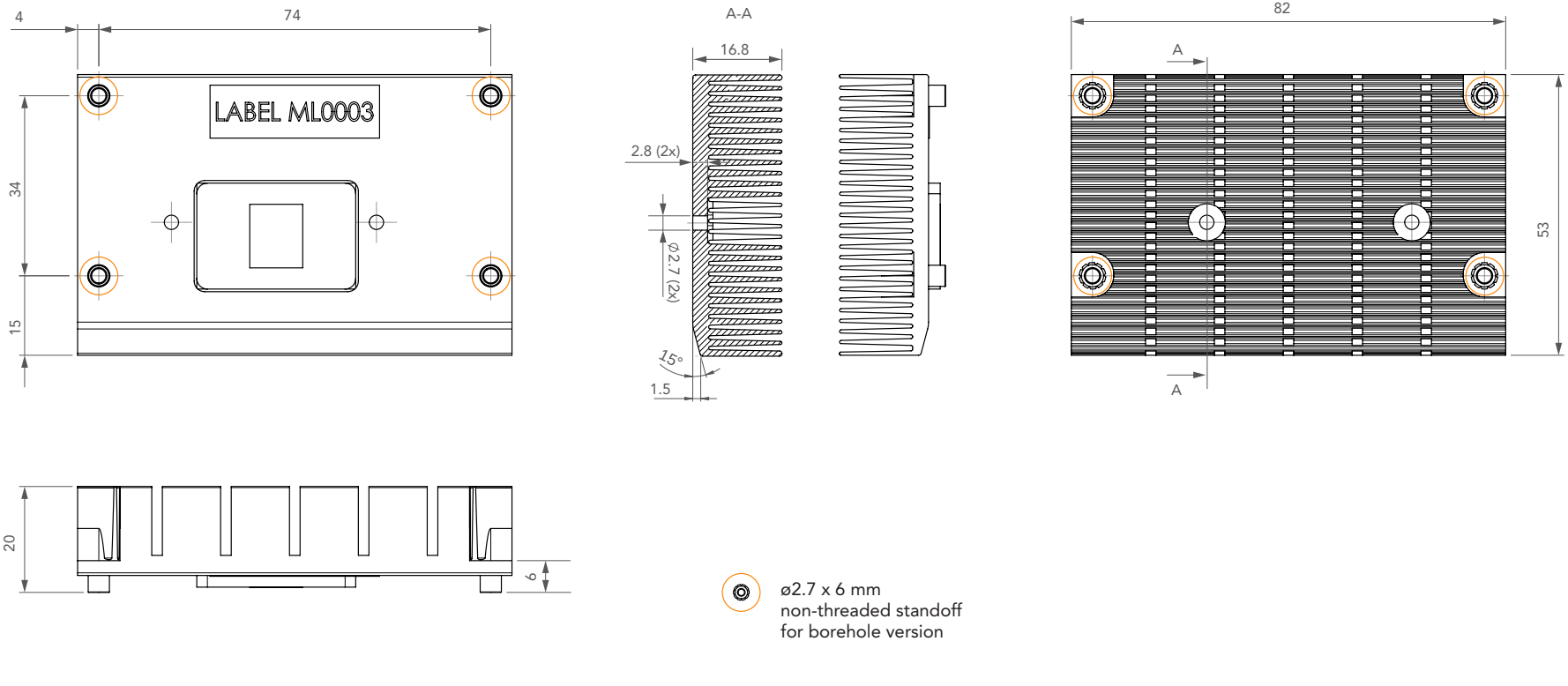
1. *The congatec heatspreaders/cooling solutions are tested only within the commercial temperature range of 0° to 60°C. Therefore, if your application that features a congatec heatspreader/cooling solution operates outside this temperature range, ensure the correct operating temperature of the module is maintained at all times. This may require additional cooling components for your final application's thermal solution.*

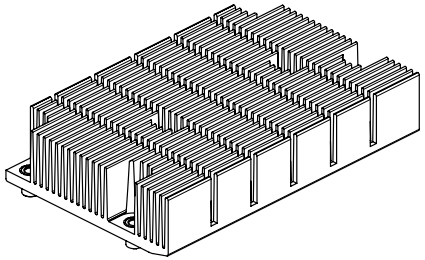
2. *For adequate heat dissipation, use the mounting holes on the cooling solution to attach it to the module. Apply thread-locking fluid on the screws if the cooling solution is used in a high shock and/or vibration environment. To prevent the standoff from stripping or cross-threading, use non-threaded carrier board standoffs to mount threaded cooling solutions.*

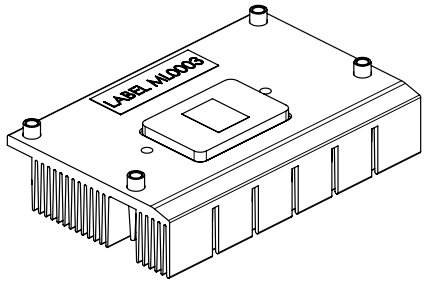
3. *For applications that require vertically-mounted cooling solution, use only coolers that secure the thermal stacks with fixing post. Without the fixing post feature, the thermal stacks may move.*

4. *Do not exceed the recommended maximum torque. Doing so may damage the module or the carrier board, or both.*

4.1 CSP Dimensions



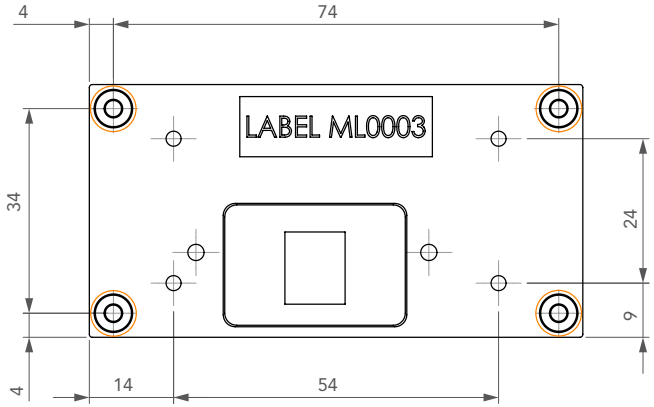


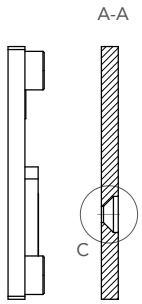


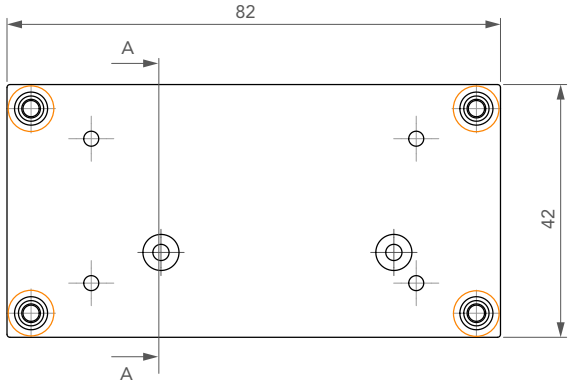
Note

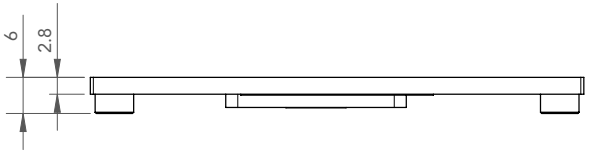
The dimensions are valid for lidded and bare-die variants.

4.2 HSP Dimensions

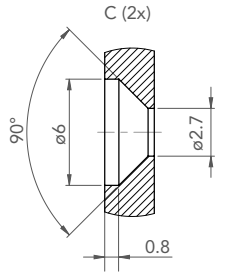


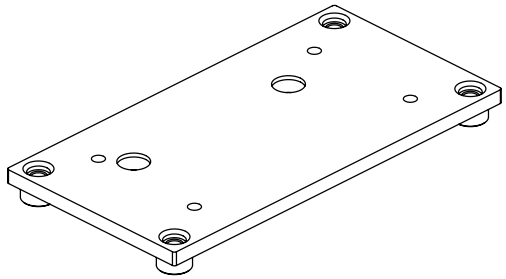


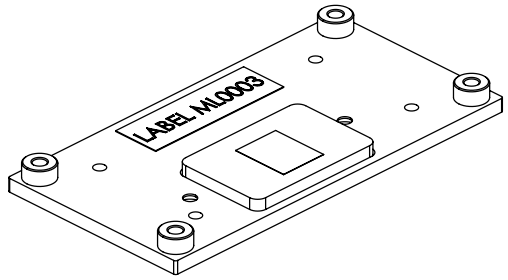




ø2.7 x 6 mm
non-threaded standoff
for borehole version







Note

The dimensions are valid for lidded and bare-die variants.

5 Connector Rows

The conga-SA5 has 314 edge fingers that mate with the MXM3 connector located on the carrier board. This connector is able to interface the signals on the conga-SA5 with the carrier board peripherals.

5.1 Display Interfaces

The conga-SA5 offers the following display interfaces:

- dual-channel LVDS
- native HDMI
- dual-mode DisplayPort (DP++)

The table below shows the display combination.

Table 8 Display Combination

	Display 1		Display 2		Display 3	
	External	Max. Resolution	External	Max. Resolution	Internal/External	Max. Resolution
Default	DP++	4096x2160 @ 60Hz	HDMI	3840x2160 @ 30Hz	LVDS	1920x1200 @ 60Hz (dual mode)
Option	DP++	4096x2160 @ 60Hz	HDMI	3840x2160 @ 30Hz	eDP/DSI	eDP: 3840x2160 @ 60 Hz DSI: 1920x1200 @ 60 Hz (1 x4 lane) or 2560x1600 @ 60 Hz (2 x4 lane)
Option	DP++	4096x2160 @ 60Hz	DP++	4096x2160 @ 60Hz	LVDS/DSI/eDP	LVDS: 1920x1200 @ 60Hz (dual mode) eDP: 3840x2160 @ 60 Hz DSI: 1920x1200 @ 60 Hz (1 x4 lane) or 2560x1600 @ 60 Hz (2 x4 lane)

5.1.1 LVDS

The conga-SA5 offers an LVDS interface on the edge finger. The interface supports:

- single- or dual-channel LVDS (color depths of 18 bpp or 24 bpp)
- integrated flat panel interface with clock frequency up to 112 MHz
- VESA and OpenLDI LVDS color mappings
- automatic panel detection via Embedded Panel Interface based on VESA EDIDTM 1.3
- resolution up to 1920x1200 in dual LVDS bus mode

Note

1. *LVDS channel A (first channel) supports an optional eDP or MIPI DSI interface (assembly option).*
2. *Variants with optional eDP or MIPI DSI interface do not support LVDS interface*
3. *Only one MIPI DSI panel is supported (maximum of two channels, with up to four lanes each)*

5.1.2 HDMI

The conga-SA5 offers a native HDMI interface. The interface supports:

- HDMI 1.4b specification
- resolutions up to 3840x2160 @ 30 Hz

Note

1. *The HDMI interface supports an optional dual-mode DisplayPort interface (assembly option).*
2. *Variants with optional dual-mode DisplayPort do not support native HDMI voltage levels.*

5.1.3 DP ++

The conga-SA5 offers a dual-mode DisplayPort (DP++). The interface supports:

- DisplayPort 1.2 specification
- resolutions up to 4096x2160 @ 60 Hz

5.2 PCI Express™

The conga-SA5 offers up to four PCI Express™ lanes. The lanes support:

- up to 5 GT/s (Gen 2) speed
- a 4 x1 link configuration (default) [1]
- optional 1 x4 or 2 x2 or 1 x2 + 2 x1 [2] link configuration (require customized BIOS firmware)
- lane polarity inversion

Note

1. *Requires a clock buffer on the carrier board.*
2. *Possible with an assembly option.*

5.2.1 Reference Clock Configuration

The conga-SA5 provides up to three PCIe reference clocks to the carrier board as described in the table below.

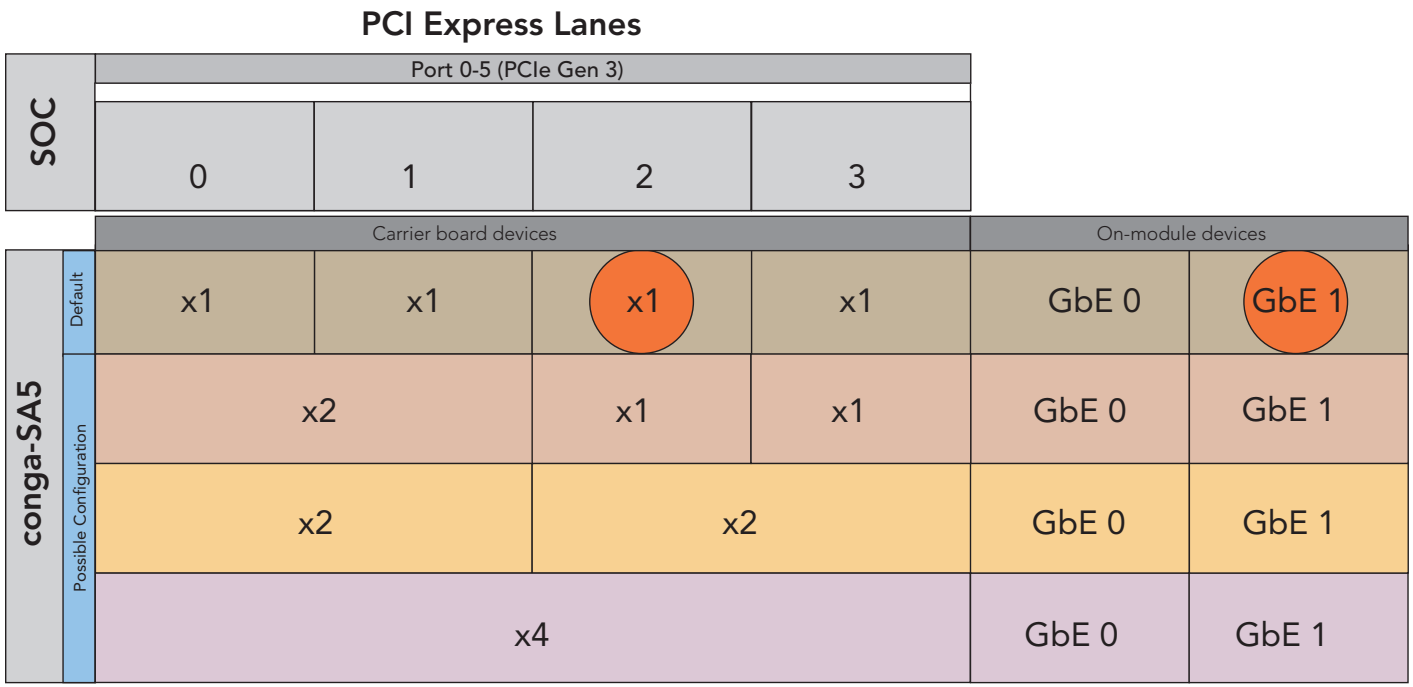
Table 9 PCIe Reference Clock Configuration

	PCIe Lanes For Carrier Board				PCIe Lanes For On-module Devices		Reference Clock Provided to Carrier Board
	PCIe0	PCIe1	PCIe2	PCIe3	PCIe4	PCIe5	
Default	x1	x1	x1	x1	Gbe0	Gbe1	PCIe_A_REFCK PCIe_B_REFCK
Option1 (disable Gbe1)	x1	x1	x1	x1	Gbe0	N.A	PCIe_A_REFCK PCIe_B_REFCK PCIe_C_REFCK
Option 2 (disable Gbe1, enable Wifi)	x1	x1	x1	x1	Gbe0	Wifi	PCIe_A_REFCK PCIe_B_REFCK
Option 3 (enable Gbe0, Gbe1 and Wifi)	x1	x1	Wifi	x1	Gbe0	Gbe1	PCIe_A_REFCK

Note

The number of reference clocks it provides depends on the number of on-module PCIe devices (Gbe, Wifi). For example, variants with one PCIe device will offer three PCIe reference clocks while variants with two on-module PCIe devices will offer two reference clocks for carrier board usage.

5.2.2 PCIe Link Configuration



Optional for onboard Wifi/BT (assembly option)

5.3 Gigabit Ethernet

The conga-SA5 offers two Gigabit Ethernet interfaces—via Intel® i210 and i211 controllers. The interfaces support full-duplex operation at 10/100/1000 Mbps and half-duplex operation at 10/100 Mbps.

5.4 SATA

The conga-SA5 offers one SATA interface on the edge finger. The interface supports:

- SATA specification 3.2
- independent DMA operation
- data transfer rates up to 6.0 Gb/s
- AHCI mode using memory space

Note

The interface does not support legacy mode using I/O space.

5.5 Universal Serial Bus (USB)

The conga-SA5 offers the following USB interfaces:

- four USB 2.0 with support for:
  - USB 1.1 and 2.0 specifications
  - up to 480 Mbps data transfer
  - high-speed, full-speed and low-speed signalling
  - additional two ports if SuperSpeed ports are not implemented
- two USB 3.0/2.0 with support for:
  - USB 3.0 specification
  - up to 5 Gbps data transfer
  - SuperSpeed, high-speed, full-speed and low-speed signalling
  - optional dual-role support on USB port 3 (assembly option)

Table 10 Possible USB Port Mapping

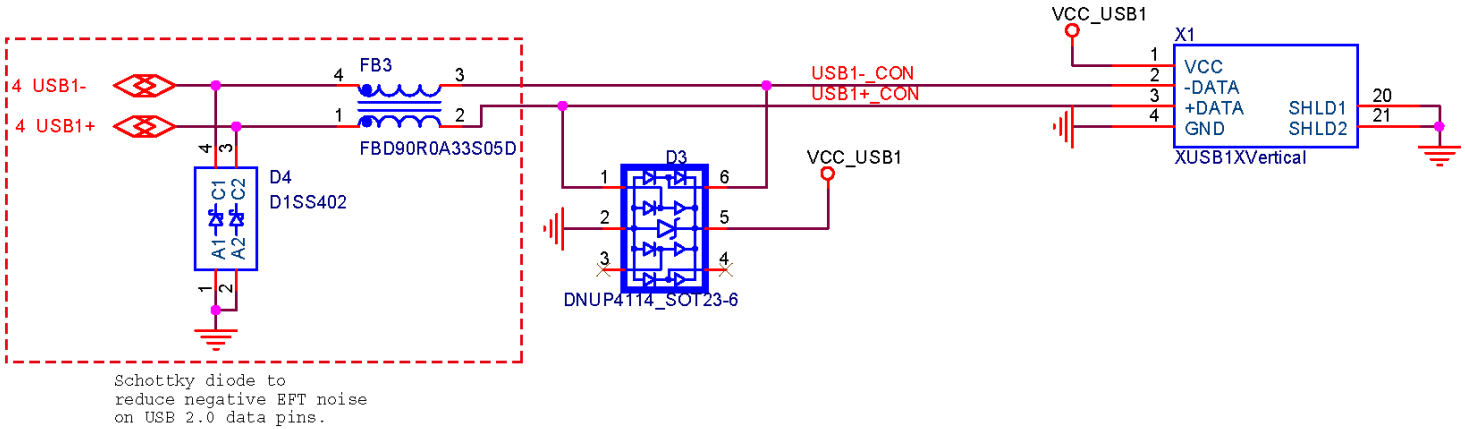
	USB 2.0		USB 3.0/2.0	
	Host Only	Dual Role	Host Only	Dual Role
Default	3 ports	1 port	2 port	-
Option	4 ports	-	1 port	1 port
Option	4 ports	-	2 ports	-
Option	6 ports	-	-	-

Note

For USB 3.0 support on your carrier board, pair USB 2.0 port 2 or 3 or both with the SuperSpeed signals.

Caution

To pass the Electrical Fast Transient (EFT) test, you must add a schottky diode (1SS402 or equivalent) to all USB 2.0 data lanes routed to a connector on your carrier board. The schottky diode must be placed before the common-mode choke as shown below:



5.6 SD Card

The conga-SA5 offers a 4-bit SD interface on the edge finger. The interface supports:

- SD Memory Card Specification 3.01
- SD 3.01 @ 1.8 V or @ 3.3 V signaling
- up to 200 MHz clock frequency
- up to 104 MBps data rates with four parallel data lines
- 1-bit and 4-bit transfer mode
- card insertion and removal detection

Note

The SD card interface supports only storage devices.

5.7 Audio (HDA)

The conga-SA5 offers up to one HDA interface.

Note

1. *GPIO functionality on GPIO4 is not supported if HDA interface is implemented.*
2. *The I2S interface is not supported.*

5.8 UART

The conga-SA5 provides four UART ports:

- UART0 and UART2 via the SoC [1,2]
- UART1 and UART3 (without handshake signals) via the congatec board controller [1,2]

Note

1. *The validated Intel HSUART driver for Windows 10 and the congatec board controller UART driver is available on the congatec website*
2. *No support for legacy mode operation*

5.9 GPIO

The conga-SA5 offers five non-multiplexed GPIOs (port 7 - port 11) by default. The GPIOs are controlled by the congatec Board controller.

5.10 SPI

The conga-SA5 offers two SPI interfaces:

- eSPI/SPI1 for a general purpose SPI device
- SPI0 for on-module flash device, carrier board flash device or SPI TPM device [1,2]

Note

1. *Use only SPI0_CS1# (pin P31) for SPI TPM device*
2. *A custom BIOS is required for SPI TPM support*

5.11 I2C

The conga-SA5 offers two I2C interfaces:

- general purpose I2C
- power management I2C

These interfaces are implemented through the congatec board controller and accessed through the congatec CGOS driver and API. The controller provides a fast-mode multi-master I2C bus that has maximum I2C bandwidth.

5.12 Power Control

The conga-SA5 operates only with 5 V input voltage. Its power-up sequence is described below:

1. The 5 V input voltage (VDD_IN) supplied to the carrier board powers the conga-SA5.
2. The conga-SA5 enables its power circuits if the VIN_PWR_BAD# signal is high.
3. Depending on the carrier board design and configuration, the conga-SA5 detects a power button event (PWRBTN#) if implemented.

4. The conga-SA5 enables the carrier board power by asserting CARRIER_PWR_ON (SUS_S5#) and CARRIER_STBY# (SUS_S3#).

5. The conga-SA5 releases the RESET_OUT# and starts the boot process.

The power control signals are described below:

VIN_PWR_BAD#

When the VIN_PWR_BAD# signal (pin S150) is low, it indicates that the input voltage to the conga-SA5 is either not ready or out of specified range. Carrier board hardware should drive this signal low until the input power is up and stable. Releasing VIN_PWR_BAD# too early can cause numerous boot up problems.

CARRIER_PWR_ON

The CARRIER_PWR_ON signal (pin S154) is an active-high output signal. The module asserts this signal when all its power supplies are up, and subsequently enables the carrier board power supplies. This signal is equivalent to ACPI SUS_S5# signal.

CARRIER_STBY#

The CARRIER_STBY# signal (pin S153) is an active-low output that can be used to indicate that the conga-SA5 is going into suspend state, where only power management functions and system memory are powered.

The CARRIER_STBY# signal can also be used to disable the carrier board power that is not required during standby.

RESET_IN#

The RESET_IN# signal (pin P127) is an active-low open drain input signal from the carrier board. The signal may be used to force the module to reset or reboot.

RESET_OUT#

The RESET_OUT# signal (pin P126) is an active-low output signal from the module. The module asserts this signal during the power-up sequencing to allow the carrier board power circuits to come up. The module deasserts this signal to begin the boot-up process.

POWER_BTN#

The POWER_BTN# (pin P128) is an active-low open drain power button input from the carrier board. This power button signal is used to wake up or shut down the system from S5 state (soft off).

Power Supply Implementation Guidelines

The operational power source for the conga-SA5 is 5 V. The remaining necessary voltages are internally generated on the module with onboard voltage regulators.

Note

When designing a power supply for a conga-SA5 application, be aware that the system may malfunction when a 5V power supply that produces non-monotonic voltage is used to power the system up. Though this problem is rare, it has been observed in some mobile power supply applications.

The problem is that some internal circuits on the module (e.g. clock-generator chips) generate their own reset signals when the supply voltage exceeds a certain voltage threshold. A voltage dip after passing this threshold may lead to these circuits becoming confused, thereby resulting in a malfunction.

To ensure this problem does not occur, observe the power supply rise waveform through an oscilloscope, during the power supply qualication phase. This will help to determine if the rise is indeed monotonic and does not have any dips. For more information, see the "Power Supply Design Guide for Desktop Platform Form Factors" document at www.intel.com.

Inrush and Maximum Current Peaks on VDD_IN

The maximum peak-current on the conga-SA5 VDD_IN (5 V) power rail can be as high as 5 A for a maximum of 100 µs. You should therefore ensure the power supply and decoupling capacitors provide enough power to drive the module.

Note

For more information about power control event signals, refer to the SMARC® specification.

6 Additional Features

6.1 Optional Onboard Interfaces

The conga-SA5 offers the following optional interfaces:

- Wi-fi/Bluetooth module
- Discrete TPM 2.0 via the LPC bus

Note

The conga-SA5 variant with part number 050031 has a discrete TPM (Infineon SLB9665VQ2.0) and an onboard Wi-fi/Bluetooth module by default.

6.2 eMMC 5.0

The conga-SA5 supports up to 64 GB eMMC 5.0 flash. Changes to the onboard eMMC may occur during the lifespan of the module in order to keep up with the rapidly changing eMMC technology.

The performance of the newer eMMC may vary depending on the eMMC technology.

Note

For adequate operation of the eMMC, ensure that at least 15 % of the eMMC storage is reserved for vendor-specific functions."

6.3 TPM 2.0

The conga-SA5 offers a firmware-based TPM 2.0 (Intel PTT) by default, as well as an option to integrate a discrete TPM 2.0 via the LPC bus.

Note

1. *Only the variant with part number 050031 has a discrete TPM by default.*
2. *You cannot use both the firmware TPM and the discrete TPM at the same time.*
3. *To use the discrete TPM, disable the firmware-based TPM in the BIOS setup menu via the Advanced -> Platform Trust Technology -> fTPM submenu. Save the changes and exit to complete the system configuration changes.*

6.4 congatec Board Controller (cBC)

The conga-SA5 is equipped with a microcontroller. The microcontroller plays an important role for most of the congatec BIOS features. By isolating some of the embedded features such as system monitoring or the I²C bus from the x86 core architecture, the microcontroller increases the performance and reliability of the BIOS features, even during low power mode. In addition, it ensures the congatec embedded feature set is compatible amongst all congatec modules.

Some of the features offered by the cBC are described below:

6.4.1 Board Information

The cBC provides a rich data-set of manufacturing and board information such as serial number, EAN number, hardware and firmware revisions, and so on. It also keeps track of dynamically changing data like runtime meter and boot counter.

6.4.2 General Purpose Input/Output

The conga-SA5 offers general purpose inputs and outputs for custom system design. These GPIOs are controlled by the cBC.

6.4.3 Fan Control

The cBC uses the PWM (FAN_PWMOUT) signal to adjust the rotational speed of the fan without changing the fan's input voltage. Additionally, the FAN_TACHOIN signal provides the ability to monitor the system's fan RPMs (revolutions per minute).

For accurate RPM reading, the FAN_TACHOIN signal must receive two pulses per revolution. Therefore, a two pulse per revolution fan or similar hardware solution is recommended.

Note

1. *Use a four-wire fan to generate the correct speed readout. For the correct fan control (PWMOUT, TACHIN) implementation, see the SMARC Design Guide Specification.*

2. *PWMOUT and TACHIN share their pins with GPIO 5 and 6 respectively. The conga-SA5 does not support fan control if these pins are used for GPIO functionality.*

6.4.4 Power Loss Control

The cBC has full control of the power-up of the module and therefore can be used to specify the behavior of the system after an AC power loss condition. Supported modes are “Always On”, “Remain Off” and “Last State”.

6.4.5 Watchdog

The conga-SA5 is equipped with a multi stage watchdog solution that is triggered by software. The conga-SA5 does not support external hardware triggering because the SMARC Specification does not provide support for external hardware triggering of the watchdog. For more information, see the application note AN3_Watchdog.pdf on the congatec GmbH website at www.congatec.com.

Note

The conga-SA5 module does not support the watchdog NMI mode.

6.5 OEM BIOS Customization

The conga-SA5 is equipped with congatec Embedded BIOS, which is based on American Megatrends Inc. Aptio UEFI firmware. The congatec Embedded BIOS allows system designers to modify the BIOS. For more information about customizing the congatec Embedded BIOS, refer to the congatec System Utility user’s guide CGUTLm1x.pdf on the congatec website at www.congatec.com or contact technical support.

The customizable features are described below:

6.5.1 OEM Default Settings

This feature allows system designers to create and store their own BIOS default configuration. Customized BIOS development by congatec for OEM default settings is no longer necessary because customers can easily perform this configuration by themselves using the congatec system utility CGUTIL. See congatec application note AN8_Create_OEM_Default_Map.pdf on the congatec website for details on how to add OEM default settings to the congatec Embedded BIOS.

6.5.2 OEM Boot Logo

This feature allows system designers to replace the standard text output displayed during POST with their own BIOS boot logo. Customized BIOS development by congatec for OEM Boot Logo is no longer necessary because customers can easily perform this configuration by themselves using the congatec system utility CGUTIL. See congatec application note AN8_Create_And_Add_Bootlogo.pdf on the congatec website for details on how to add OEM boot logo to the congatec Embedded BIOS.

6.5.3 OEM POST Logo

This feature allows system designers to replace the congatec POST logo displayed in the upper left corner of the screen during BIOS POST with their own BIOS POST logo. Use the congatec system utility CGUTIL 1.5.4 or later to replace/add the OEM POST logo.

6.5.4 OEM BIOS Code/Data

With the congatec embedded BIOS, system designers can add their own code to the BIOS POST process. The congatec Embedded BIOS first calls the OEM code before handing over control to the OS loader.

Note

The OEM BIOS code of the new UEFI based firmware is called only when the CSM (Compatibility Support Module) is enabled in the BIOS setup menu. For more information on how to add OEM code, contact congatec technical support.

6.5.5 OEM DXE Driver

This feature allows designers to add their own UEFI DXE driver to the congatec embedded BIOS. Contact congatec technical support for more information on how to add an OEM DXE driver.

6.6 congatec Battery Management Interface

To facilitate the development of battery powered mobile systems based on embedded modules, congatec GmbH defined an interface for the exchange of data between a CPU module (using an ACPI operating system) and a Smart Battery system. A system developed according to the congatec Battery Management Interface Specification can provide the battery management functions supported by an ACPI capable operating system (e.g. charge state of the battery, information about the battery, alarms/events for certain battery states, ...) without the need for any additional modifications to the system BIOS.

In addition to the ACPI-Compliant Control Method Battery mentioned above, the latest versions of the conga-SA5 BIOS and board controller firmware also support LTC1760 battery manager from Linear Technology and a battery only solution (no charger). All three battery solutions are supported on the I2C bus and the SMBus. This gives the system designer more flexibility when choosing the appropriate battery sub-system.

For more information about the supported Battery Management Interface, contact your local sales representative.

6.7 API Support (CGOS)

In order to benefit from the above mentioned non-industry standard feature set, congatec provides an API that allows application software developers to easily integrate all these features into their code. The CGOS API (congatec Operating System Application Programming Interface) is the congatec proprietary API that is available for all commonly used Operating Systems such as Win32, Win64, Win CE, Linux.

The architecture of the CGOS API driver provides the ability to write application software that runs unmodified on all congatec CPU modules. All the hardware related code is contained within the congatec embedded BIOS on the module. See section 1.1 of the CGOS API software developers guide, which is available on the congatec website.

6.8 congatec System Sensors

The conga-SA5 offers the following sensors and monitors:

- temperature sensors
  - CPU temperature based on CPU Digital Thermal Sensor
  - Board temperature sensor located on the Board Controller
- voltage sensors
  - 5V standard voltage sensor
  - 5V standby voltage sensor
- current sensor
- fan monitor

The sensors and monitors are accessible through CGOS interface, and also visible on the “Health Monitor”submenu in the BIOS Setup.

6.9 Suspend to Ram

The Suspend to RAM feature is available on the conga-SA5.

7 conga Tech Notes

The conga-SA5 has some technological features that require additional explanation. The following section will give the reader a better understanding of some of these features.

7.1 Intel® Apollo Lake SoC Features

7.1.1 Processor Core

The SoC features Dual or Quad Out-of-Order Execution processor cores. The cores are grouped into Dual-Core modules with each module sharing a 1 MB L2 cache (512 KB per core). Some of the features supported by the core are:

- Intel® 64 architecture
- Intel® Streaming SIMD Extensions
- Support for Intel® VTx-2 and VT-d
- Thermal management support vial Intel® Thermal Monitor
- Uses Power Aware Interrupt Routing
- Uses 14 nm process technology

Note

Intel® Hyper-Threading technology is not supported (four cores execute four threads)

7.1.1.1 Intel® Virtualization Technology

Intel® Virtualization Technology (Intel® VT) makes a single system appear as multiple independent systems to software. With this technology, multiple, independent operating systems can run simultaneously on a single system. The technology components support virtualization of platforms based on Intel architecture microprocessors and chipsets. Intel® Virtualization Technology for IA-32, Intel® 64 and Intel® Architecture (Intel® VT-x) added hardware support in the processor to improve the virtualization performance and robustness.

RTS Real-Time Hypervisor supports Intel® VT and is verified on all current congatec x86 hardware.

Note

congatec supports RTS Hypervisor.

7.1.1.2 AHCI

The SoC provides hardware support for Advanced Host Controller Interface (AHCI), a programming interface for SATA host controllers. Platforms supporting AHCI may take advantage of performance features such as no master/slave designation for SATA devices (each device is treated as a master) and hardware-assisted native command queuing. AHCI also provides usability enhancements such as Hot-Plug.

7.1.1.3 Thermal Management

ACPI is responsible for allowing the operating system to play an important part in the system's thermal management. This results in the operating system having the ability to take control of the operating environment by implementing cooling decisions according to the demands put on the CPU by the application.

The conga-SA5 ACPI thermal solution offers two different cooling policies.

- **Passive Cooling**

When the temperature in the thermal zone must be reduced, the operating system can decrease the power consumption of the processor by throttling the processor clock. One of the advantages of this cooling policy is that passive cooling devices (in this case the processor) do not produce any noise. Use the "passive cooling trip point" setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to start or stop the passive cooling procedure.

- **Critical Trip Point**

If the temperature in the thermal zone reaches a critical point then the operating system will perform a system shut down in an orderly fashion in order to ensure that there is no damage done to the system as result of high temperatures. Use the "critical trip point" setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to shut down the system.

Note

The end user must determine the cooling preferences for the system by using the setup nodes in the BIOS setup program to establish the appropriate trip points.

If passive cooling is activated and the processor temperature is above the trip point the processor clock is throttled. See section 12 of the ACPI Specification 2.0 C for more information about passive cooling.

7.2 ACPI Suspend Modes and Resume Events

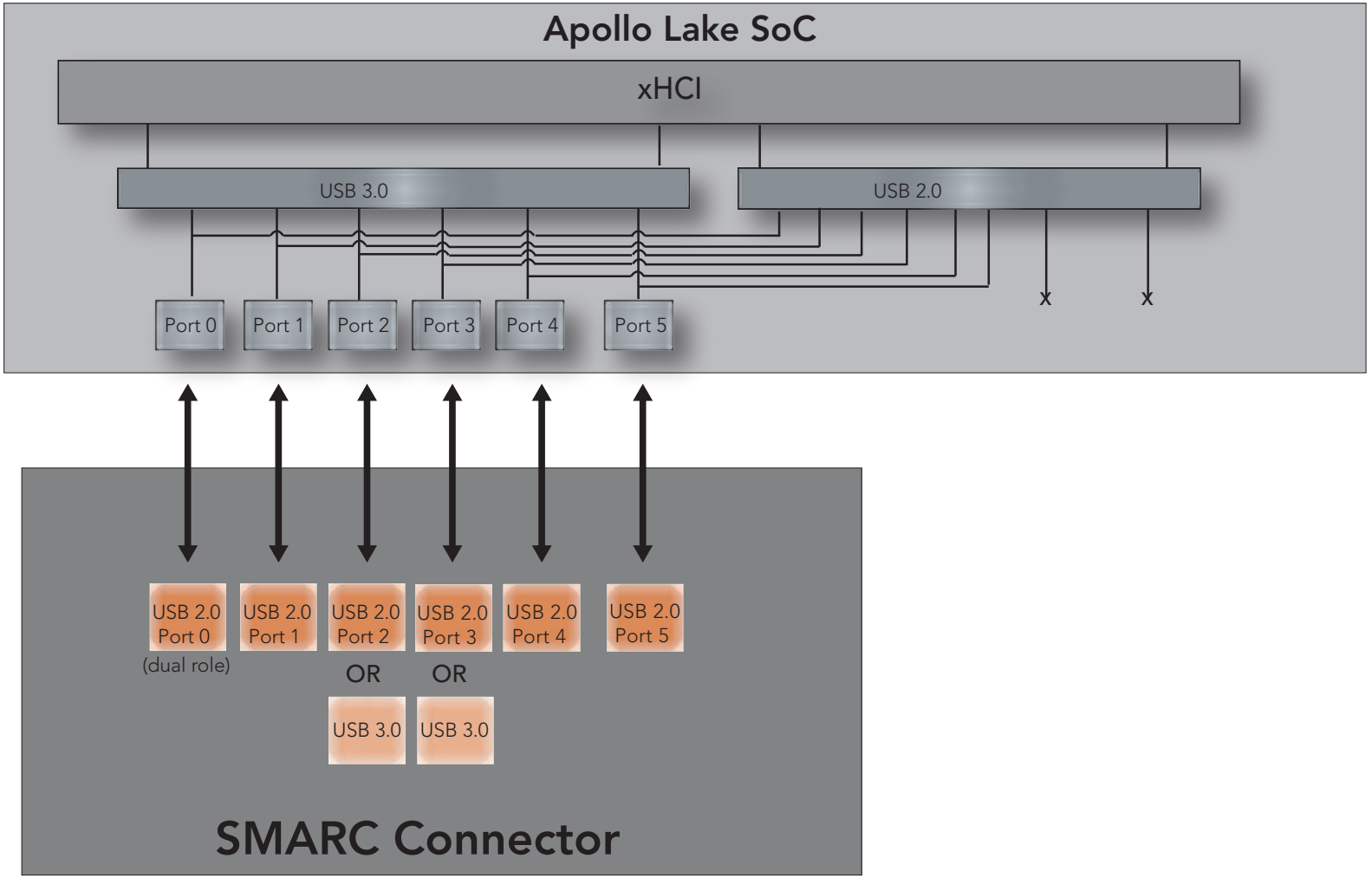
The conga-SA5 BIOS supports S3 (Suspend to RAM). The BIOS does not support S4 (Suspend to Disk) even though the Windows 10 and Linux support it.

Table 11 Wake Events

The table below lists the events that wake the system from S3.

Wake Event	Conditions or remarks
Power Button	Wakes unconditionally from S3-S5
Onboard LAN Event	Device driver must be configured for Wake On LAN support
SMBALERT#	Wakes unconditionally from S3-S5
PCI Express WAKE#	Wakes unconditionally from S3-S5
WAKE#	Wakes unconditionally from S3
USB Mouse/Keyboard Event	When standby mode is set to S3, the standby power source must power the USB hardware: • in the ACPI setup menu, set "USB Device Wakeup" to "Enabled" (if setup node is available in the BIOS setup menu) • in Device Manager, expand "Keyboard" or "Mice and other pointing devices" • right-click keyboard or mouse device and click "Properties" • click "Power Management" tab and check "Allow this device to wake the computer'
RTC Alarm	In the power setup menue, active and configure "Resume On RTC Alarm" (only available in S5)
Watchdog Power Button Event	Wakes unconditionally from S3-S5

7.3 USB Port Mapping



8 Signal Descriptions and Pinout Tables

The following section describes the signals found on SMARC® module's edge fingers. The pinout of the module complies with SMARC Specification 2.1.

The table below describes the terminology used in this section. The PU/PD column indicates if a pull-up or pull-down resistor has been used. If the field entry area in this column for the signal is empty, then no pull-up or pull-down resistor has been implemented. The "#" symbol at the end of the signal name indicates that the active or asserted state occurs when the signal is at a low voltage level.

Note

Not all the signals described in this section are available on all conga-SA5 variants. Use the article number of the module and refer to the "conga-SA5 Options Information" table in section 1 to determine the options available on the module.

Table 12 Signal Tables Terminology Descriptions

Term	Description
I	Input to the module
O	Output from the module
O OD	Open drain output from the module
I OD	Open drain input to the module, with pull-up on module
OD	Open drain
I/O	Bi-directional Input/Output Pin
PU(i)/PD(i)	Pull-up or pull-down resistor internal to the SoC or transceiver
VDD_IN	Signal may be exposed to module input voltage range (4.75 to 5.25V)
CMOS	Logic input or output with 3.3 V signal level
GBe MDI	Differential analog signaling for Gigabit Media Dependent Interface
LVDS DP	LVDS signaling for DisplayPort devices
LVDS D-PHY	LVDS signaling for MIPI CSI-2 camera and DSI display interfaces
LVDS LCD	LVDS signaling for LVDS LCD displays
LVDS PCIE	LVDS signaling for PCIe interfaces
LVDS SATA	LVDS signaling for SATA interfaces
TMDS	LVDS signaling for HDMI display interfaces
USB	DC coupled differential signaling for traditional (non-Superspeed) USB signals
USB SS	LVDS signaling for SuperSpeed USB signals
PCIE	PCI Express differential pair signals. In compliance with the PCI Express Base Specification 2.0
USB VBUS 5V	5V tolerant input for USB VBUS detection

Table 13 SMARC Edge Finger Pinout

P-PIN	Primary (Top) Side	S-Pin	Secondary (Bottom) Side
		S1	CSI1_TX+ / I2C_CAM1_CK
P1	SMB_ALERT_1V8#	S2	CSI1_TX- / I2C_CAM1_DAT
P2	GND	S3	GND
P3	CSI1_CK+	S4	RSVD
P4	CSI1_CK-	S5	CSI0_TX+ / I2C_CAM0_CK
P5	GBE1_SDP	S6	CAM_MCK
P6	GBE0_SDP	S7	CSI0_TX- / I2C_CAM0_DAT
P7	CSI1_RX0+	S8	CSI0_CK+
P8	CSI1_RX0-	S9	CSI0_CK-
P9	GND	S10	GND
P10	CSI1_RX1+	S11	CSI0_RX0+
P11	CSI1_RX1-	S12	CSI0_RX0-
P12	GND	S13	GND
P13	CSI1_RX2+	S14	CSI0_RX1+
P14	CSI1_RX2-	S15	CSI0_RX1-
P15	GND	S16	GND
P16	CSI1_RX3+	S17	GBE1_MDI0+
P17	CSI1_RX3-	S18	GBE1_MDI0-
P18	GND	S19	GBE1_LINK100#
P19	GBE0_MDI3-	S20	GBE1_MDI1+
P20	GBE0_MDI3+	S21	GBE1_MDI1-
P21	GBE0_LINK100#	S22	GBE1_LINK1000#
P22	GBE0_LINK1000#	S23	GBE1_MDI2+
P23	GBE0_MDI2-	S24	GBE1_MDI2-
P24	GBE0_MDI2+	S25	GND
P25	GBE0_LINK_ACT#	S26	GBE1_MDI3+
P26	GBE0_MDI1-	S27	GBE1_MDI3-
P27	GBE0_MDI1+	S28	GBE1_CTREF
P28	GBE0_CTREF	S29	PCIE_D_TX+
P29	GBE0_MDI0-	S30	PCIE_D_TX-
P30	GBE0_MDI0+	S31	GBE1_LINK_ACT#
P31	SPI0_CS1#	S32	PCIE_D_RX+

P-PIN	Primary (Top) Side	S-Pin	Secondary (Bottom) Side
P32	GND	S33	PCIE_D_RX-
P33	SDIO_WP	S34	GND
P34	SDIO_CMD	S35	USB4+
P35	SDIO_CD#	S36	USB4-
P36	SDIO_CK	S37	USB3_VBUS_DET
P37	SDIO_PWR_EN	S38	AUDIO_MCK
P38	GND	S39	I2S0_LRCK [2]
P39	SDIO_D0	S40	I2S0_SDOUT [2]
P40	SDIO_D1	S41	I2S0_SDIN [2]
P41	SDIO_D2	S42	I2S0_CK [2]
P42	SDIO_D3	S43	ESPI_ALERT0# [1]
P43	SPI0_CS0#	S44	ESPI_ALERT1# [1]
P44	SPI0_CK	S45	RSVD
P45	SPI0_DIN	S46	RSVD
P46	SPI0_DO	S47	GND
P47	GND	S48	I2C_GP_CK
P48	SATA_TX+	S49	I2C_GP_DAT
P49	SATA_TX-	S50	HDA_SYNC
P50	GND	S51	HDA_SDO
P51	SATA_RX+	S52	HDA_SDI
P52	SATA_RX-	S53	HDA_CK
P53	GND	S54	SATA_ACT#
P54	ESPI_CS0#	S55	USB5_EN_OC#
P55	ESPI_CS1# [1]	S56	ESPI_IO_2 [1]
P56	ESPI_CK	S57	ESPI_IO_3 [1]
P57	ESPI_IO_1	S58	ESPI_RESET# [1]
P58	ESPI_IO_0	S59	USB5+
P59	GND	S60	USB5-
P60	USB0+	S61	GND
P61	USB0-	S62	USB3_SSTX+
P62	USB0_EN_OC#	S63	USB3_SSTX-
P63	USB0_VBUS_DET	S64	GND
P64	USB0_OTG_ID	S65	USB3_SSRX+
P65	USB1+	S66	USB3_SSRX-

P-PIN	Primary (Top) Side	S-Pin	Secondary (Bottom) Side
P66	USB1-	S67	GND
P67	USB1_EN_OC#	S68	USB3+
P68	GND	S69	USB3-
P69	USB2+	S70	GND
P70	USB2-	S71	USB2_SSTX+
P71	USB2_EN_OC#	S72	USB2_SSTX-
P72	RSVD	S73	GND
P73	RSVD	S74	USB2_SSRX+
P74	USB3_EN_OC#	S75	USB2_SSRX-
	Key		Key
P75	PCIE_A_RST#	S76	PCIE_B_RST#
P76	USB4_EN_OC#	S77	PCIE_C_RST#
P77	RSVD	S78	PCIE_C_RX+
P78	RSVD	S79	PCIE_C_RX-
P79	GND	S80	GND
P80	PCIE_C_REFCK+	S81	PCIE_C_TX+
P81	PCIE_C_REFCK-	S82	PCIE_C_TX-
P82	GND	S83	GND
P83	PCIE_A_REFCK+	S84	PCIE_B_REFCK+
P84	PCIE_A_REFCK-	S85	PCIE_B_REFCK-
P85	GND	S86	GND
P86	PCIE_A_RX+	S87	PCIE_B_RX+
P87	PCIE_A_RX-	S88	PCIE_B_RX-
P88	GND	S89	GND
P89	PCIE_A_TX+	S90	PCIE_B_TX+
P90	PCIE_A_TX-	S91	PCIE_B_TX-
P91	GND	S92	GND
P92	HDMI_D2+ / DP1_LANE0+	S93	DP0_LANE0+
P93	HDMI_D2- / DP1_LANE0-	S94	DP0_LANE0-
P94	GND	S95	DP0_AUX_SEL
P95	HDMI_D1+ / DP1_LANE1+	S96	DP0_LANE1+

P-PIN	Primary (Top) Side	S-Pin	Secondary (Bottom) Side
P96	HDMI_D1- / DP1_LANE1-	S97	DP0_LANE1-
P97	GND	S98	DP0_HPD
P98	HDMI_D0+ / DP1_LANE2+	S99	DP0_LANE2+
P99	HDMI_D0- / DP1_LANE2-	S100	DP0_LANE2-
P100	GND	S101	GND
P101	HDMI_CK+ / DP1_LANE3+	S102	DP0_LANE3+
P102	HDMI_CK- / DP1_LANE3-	S103	DP0_LANE3-
P103	GND	S104	USB3_OTG_ID
P104	HDMI_HPD / DP1_HPD	S105	DP0_AUX+
P105	HDMI_CTRL_CK / DP1_AUX+	S106	DP0_AUX-
P106	HDMI_CTRL_DAT / DP1_AUX-	S107	LCD1_BKLT_EN
P107	DP1_AUX_SEL	S108	LVDS1_CK+ / eDP1_AUX+ / DSI1_CLK+
P108	GPIO0 / CAM0_PWR#	S109	LVDS1_CK- / eDP1_AUX- / DSI1_CLK-
P109	GPIO1 / CAM1_PWR#	S110	GND
P110	GPIO2 / CAM0_RST#	S111	LVDS1_0+ / eDP1_TX0+ / DSI1_D0+
P111	GPIO3 / CAM1_RST#	S112	LVDS1_0- / eDP1_TX0- / DSI1_D0-
P112	GPIO4 / HDA_RST#	S113	eDP1_HPD / DSI1_TE
P113	GPIO5 / PWM_OUT	S114	LVDS1_1+ / eDP1_TX1+ / DSI1_D1+
P114	GPIO6 / TACHIN	S115	LVDS1_1- / eDP1_TX1- / DSI1_D1-
P115	GPIO7	S116	LCD1_VDD_EN
P116	GPIO8	S117	LVDS1_2+ / eDP1_TX2+ / DSI1_D2+
P117	GPIO9	S118	LVDS1_2- / eDP1_TX2- / DSI1_D2-
P118	GPIO10	S119	GND
P119	GPIO11	S120	LVDS1_3+ / eDP1_TX3+ / DSI1_D3+
P120	GND	S121	LVDS1_3- / eDP1_TX3- / DSI1_D3-
P121	I2C_PM_CK	S122	LCD1_BKLT_PWM
P122	I2C_PM_DAT	S123	RSVD
P123	BOOT_SEL0#	S124	GND
P124	BOOT_SEL1#	S125	LVDS0_0+ / eDP0_TX0+ / DSI0_D0+
P125	BOOT_SEL2#	S126	LVDS0_0- / eDP0_TX0- / DSI0_D0-
P126	RESET_OUT#	S127	LCD0_BKLT_EN
P127	RESET_IN#	S128	LVDS0_1+ / eDP0_TX1+ / DSI0_D1+
P128	POWER_BTN#	S129	LVDS0_1- / eDP0_TX1- / DSI0_D1-

P-PIN	Primary (Top) Side	S-Pin	Secondary (Bottom) Side
P129	SER0_TX	S130	GND
P130	SER0_RX	S131	LVDS0_2+ / eDP0_TX2+ / DSI0_D2+
P131	SER0_RTS#	S132	LVDS0_2- / eDP0_TX2- / DSI0_D2-
P132	SER0_CTS#	S133	LCD0_VDD_EN
P133	GND	S134	LVDS0_CK+ / eDP0_AUX+ / DSI0_CLK+
P134	SER1_TX	S135	LVDS0_CK- / eDP0_AUX- / DSI0_CLK-
P135	SER1_RX	S136	GND
P136	SER2_TX	S137	LVDS0_3+ / eDP0_TX3+ / DSI0_D3+
P137	SER2_RX	S138	LVDS0_3- / eDP0_TX3- / DSI0_D3-
P138	SER2_RTS#	S139	I2C_LCD_CK
P139	SER2_CTS#	S140	I2C_LCD_DAT
P140	SER3_TX	S141	LCD0_BKLT_PWM
P141	SER3_RX	S142	RSVD
P142	GND	S143	GND
P143	CAN0_TX [1]	S144	eDP0_HPD / DSI0_TE
P144	CAN0_RX [1]	S145	WDT_TIME_OUT#
P145	CAN1_TX [1]	S146	PCIE_WAKE#
P146	CAN1_RX [1]	S147	VDD_RTC
P147	VDD_IN	S148	LID#
P148	VDD_IN	S149	SLEEP#
P149	VDD_IN	S150	VIN_PWR_BAD#
P150	VDD_IN	S151	CHARGING#
P151	VDD_IN	S152	CHARGER_PRSNT#
P152	VDD_IN	S153	CARRIER_STBY#
P153	VDD_IN	S154	CARRIER_PWR_ON
P154	VDD_IN	S155	FORCE_RECOV#
P155	VDD_IN	S156	BATLOW#
P156	VDD_IN	S157	TEST#
		S158	GND

Note

1. *Not supported*
2. *Not connected*

Table 14 LVDS Signal Description

Signals	Pins	Description	I/O	PU/PD	Comments
LVDS0_0+ LVDS0_0-	S125 S126	LVDS primary data channel, differential pair 0	O LVDS LCD		
LVDS0_1+ LVDS0_1-	S128 S129	LVDS primary data channel, differential pair 1	O LVDS LCD		
LVDS0_2+ LVDS0_2-	S131 S132	LVDS primary data channel, differential pair 2	O LVDS LCD		
LVDS0_3+ LVDS0_3-	S137 S138	LVDS primary data channel, differential pair 3	O LVDS LCD		
LVDS0_CK+ LVDS0_CK-	S134 S135	LVDS primary data channel differential clock pair	O LVDS LCD		
LVDS1_0+ LVDS1_0-	S111 S112	LVDS secondary data channel, differential pair 0	O LVDS LCD		
LVDS1_1+ LVDS1_1-	S114 S115	LVDS secondary data channel, differential pair 1	O LVDS LCD		
LVDS1_2+ LVDS1_2-	S117 S118	LVDS secondary data channel, differential pair 2	O LVDS LCD		
LVDS1_3+ LVDS1_3-	S120 S121	LVDS secondary data channel, differential pair 3	O LVDS LCD		
LVDS1_CK+ LVDS1_CK-	S108 S109	LVDS secondary data channel differential clock pair	O LVDS LCD		
Support Pins					
LCD0_VDD_EN	S133	Controls panel 0 power enable. High enables panel VDD	O 1.8V		
LCD1_VDD_EN	S116	Controls panel 1 power enable. High enables panel VDD	O 1.8V	PD 100k	Signal is not actively driven with LVDS option
LCD0_BKLT_EN	S127	Controls panel 0 backlight enable. High enables panel backlight	O 1.8V		
LCD1_BKLT_EN	S107	Controls panel 1 backlight enable. High enables panel backlight	O 1.8V	PD 100k	Signal is not actively driven with LVDS option
LCD0_BKLT_PWM	S141	Controls panel 0 backlight brightness via pulse width modulation (PWM)	O 1.8V		
LCD1_BKLT_PWM	S122	Controls panel 1 backlight brightness via pulse width modulation (PWM)	O 1.8V	PD 100k	Signal is not actively driven with LVDS option
I2C_LCD_DAT	S140	I2C data to read LCD display EDID EEPROMs. Possible EDID EEPROM address conflicts may occur if multiple displays are implemented	I/O OD 1.8V	PU 1k3	Pull-up is active only during runtime
I2C_LCD_CK	S139	I2C clock to read LCD display EDID EEPROMs	O OD 1.8V	PU 1k3	Pull-up is active only during runtime

Table 14.1 Optional LVDS / eDP Pin Sharing Signal Description

Signals	Pins	Description	I/O	PU/PD	Comments
eDP0_TX0+ eDP0_TX0-	S125 S126	eDP0 differential pair 0	O LVDS DP		AC coupling required off-module
eDP0_TX1+ eDP0_TX1-	S128 S129	eDP0 differential pair 1	O LVDS DP		AC coupling required off-module
eDP0_TX2+ eDP0_TX2-	S131 S132	eDP0 differential pair 2	O LVDS DP		AC coupling required off-module
eDP0_TX3+ eDP0_TX3-	S137 S138	eDP0 differential pair 3	O LVDS DP		AC coupling required off-module
eDP0_AUX+ eDP0_AUX-	S134 S135	eDP0 auxiliary differential pair	O LVDS DP		AC coupling required off-module
eDP1_TX0+ eDP1_TX0-	S111 S112	eDP1 differential pair 0	O LVDS DP		Not supported
eDP1_TX1+ eDP1_TX1-	S114 S115	eDP1 differential pair 1	O LVDS DP		Not supported
eDP1_TX2+ eDP1_TX2-	S117 S118	eDP1 differential pair 2	O LVDS DP		Not supported
eDP1_TX3+ eDP1_TX3-	S120 S121	eDP1 differential pair 3	O LVDS DP		Not supported
eDP1_AUX+ eDP1_AUX-	S108 S109	eDP1 auxiliary differential pair	O LVDS DP		Not supported
Support Pins					
LCD0_VDD_EN	S133	Controls panel 0 power enable. High enables panel VDD	O 1.8V		
LCD1_VDD_EN	S116	Controls panel 1 power enable. High enables panel VDD	O 1.8V	PD 100k	Signal not actively driven with eDP option
LCD0_BKLT_EN	S127	Controls panel 0 backlight enable. High enables panel backlight	O 1.8V		
LCD1_BKLT_EN	S107	Controls panel 1 backlight enable. High enables panel backlight	O 1.8V	PD 100k	Signal not actively driven with eDP option
LCD0_BKLT_PWM	S141	Controls panel 0 backlight brightness via pulse width modulation (PWM)	O 1.8V		
LCD1_BKLT_PWM	S122	Controls panel 1 backlight brightness via pulse width modulation (PWM)	O 1.8V	PD 100k	Signal not actively driven with eDP option
I2C_LCD_DAT	S140	I2C data to read LCD display EDID EEPROMs. Possible EDID EEPROM address conflicts may occur if multiple displays are implemented	I/O OD 1.8V	PU 1k3	Optional - eDP panel information is usually via the eDP auxiliary pair
I2C_LCD_CK	S139	I2C clock to read LCD display EDID EEPROMs	O 1.8V	PU 1k3	Optional - eDP panel information is usually via the eDP auxiliary pair
eDP0_HPD eDP1_HPD	S144 S113	eDP Hot Plug Detect pins	I 1.8V	PD 100k	100k PD present only on variants with eDP support

Table 14.2 Optional LVDS / DSI Pin Sharing Signal Description

Signals	Pins	Description	I/O	PU/PD	Comments
DSI0_D0+ DSI0_D0-	S125 S126	DSI0 differential pair 0	O LVDS D-PHY		
DSI0_D1+ DSI0_D1-	S128 S129	DSI0 differential pair 1	O LVDS D-PHY		
DSI0_D2+ DSI0_D2-	S131 S132	DSI0 differential pair 2	O LVDS D-PHY		
DSI0_D3+ DSI0_D3-	S137 S138	DSI0 differential pair 3	O LVDS D-PHY		
DSI0_CLK+ DSI0_CLK-	S134 S135	DSI0 clock differential pair	O LVDS D-PHY		
DSI1_D0+ DSI1_D0-	S111 S112	DSI1 differential pair 0	O LVDS D-PHY		
DSI1_D1+ DSI1_D1-	S114 S115	DSI1 differential pair 1	O LVDS D-PHY		
DSI1_D2+ DSI1_D2-	S117 S118	DSI1 differential pair 2	O LVDS D-PHY		
DSI1_D3+ DSI1_D3-	S120 S121	DSI1 differential pair 3	O LVDS D-PHY		
DSI1_CLK+ DSI1_CLK-	S108 S109	DSI1 clock differential pair	O LVDS D-PHY		
Support Pins					
LCD0_VDD_EN LCD1_VDD_EN	S133 S116	Controls the panel power enable. High enables panel VDD	O 1.8V		
LCD0_BKLT_EN LCD1_BKLT_EN	S127 S107	Controls the panel backlight enable. High enables panel backlight	O 1.8V		
LCD0_BKLT_PWM LCD1_BKLT_PWM	S141 S122	Controls the panel backlight brightness via pulse width modulation (PWM)	O 1.8V		
I2C_LCD_DAT	S140	I2C data to read LCD display EDID EEPROMs. Possible EDID EEPROM address conflicts may occur if multiple displays are implemented	I/O OD 1.8V	PU 1k3	
I2C_LCD_CK	S139	I2C clock to read LCD display EDID EEPROMs	O 1.8V	PU 1k3	
DSI0_TE DSI1_TE	S144 S113	DSI tearing effect signal	I 1.8V		

Table 15 HDMI Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
HDMI_D0+ HDMI_D0-	P98 P99	TMDS / HDMI differential data pair 0	O TMDS		
HDMI_D1+ HDMI_D1-	P95 P96	TMDS / HDMI differential data pair 1	O TMDS		
HDMI_D2+ HDMI_D2-	P92 P93	TMDS / HDMI differential data pair 2	O TMDS		
HDMI_CK+ HDMI_CK-	P101 P102	TMDS / HDMI differential clock pair	O TMDS		
HDMI_HPD	P104	HDMI Hot plug active high detection signal that serves as an interrupt request	I 1.8V	PD 1M	
HDMI_CTRL_DAT	P106	I2C data line dedicated to HDMI	I/O 1.8V OD	PU 100k	Level shifter FET and 5V PU resistor shall be placed between the module and the HDMI connector
HDMI_CTRL_CK	P105	I2C clock line dedicated to HDMI	O 1.8V OD	PU 100k	Level shifter FET and 5V PU resistor shall be placed between the module and the HDMI connector

Note

For HDMI operation, drive DP1_AUX_SEL (pin P107) to 1.8 V on the carrier board.

Table 15.1 DP++ Operation Over HDMI Pins Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
DP1_LANE0+ DP1_LANE0-	P92 P93	DisplayPort differential data pair 0	LVDS DP		AC coupled off module
DP1_LANE1+ DP1_LANE1-	P95 P96	DisplayPort differential data pair 1	LVDS DP		AC coupled off module
DP1_LANE2+ DP1_LANE2-	P98 P99	DisplayPort differential data pair 2	LVDS DP		AC coupled off module
DP1_LANE3+ DP1_LANE3-	P101 P102	DisplayPort differential data pair 3	LVDS DP		AC coupled off module
DP1_HPD	P104	DisplayPort Hot Plug Detect	I 1.8V	PD 1M	
DP1_AUX+ DP1_AUX-	P105 P106	DisplayPort auxiliary differential pair. Used for link management and device control	I/O 1.8V OD	PU 100k	AC coupled on module
DP1_AUX_SEL	P107	Pull to GND on carrier for DP operation in dual-mode (DP++) implementations. Drive to 1.8V on carrier for HDMI operation. Terminated on module through 1M resistor to GND	I 1.8V	PD 1M	

Note

The conga-SA5 offers this interface via an assembly option.

Table 16 DisplayPort++

Signal	Pin #	Description	I/O	PU/PD	Comment
DP0_LANE0+ DP0_LANE0-	S93 S94	DisplayPort differential data pair 0	LVDS DP		AC coupled off module
DP0_LANE1+ DP0_LANE1-	S96 S97	DisplayPort differential data pair 1	LVDS DP		AC coupled off module
DP0_LANE2+ DP0_LANE2-	S99 S100	DisplayPort differential data pair 2	LVDS DP		AC coupled off module
DP0_LANE3+ DP0_LANE3-	S102 S103	DisplayPort differential data pair 3	LVDS DP		AC coupled off module
DP0_HPD	S98	DisplayPort Hot Plug Detect	I 1.8V	PD 1M	
DP0_AUX+	S105	DisplayPort auxiliary differential pair. Used for link management and device control	LVDS PCIE	PD 100k	AC coupled on module
DP0_AUX-	S106		LVDS PCIE	PU 100k	AC coupled on module
DP0_AUX_SEL	S95	Pulled to GND on carrier for DP operation in dual-mode (DP++) implementations	I 1.8V	PD 1M	

Table 17 MIPI CSI-2/-3

Signal	Pin #	Description	I/O	PU/PD	Comment
CSI0_RX0+ CSI0_RX0-	S11 S12	CSI0 differential data pair 0	I LVDS D-PHY		
CSI0_RX1+ CSI0_RX1-	S14 S15	CSI0 differential data pair 1	I LVDS D-PHY		
CSI0_CK+ CSI0_CK-	S8 S9	CSI0 differential clock pair	I LVDS D-PHY		
CAM0_PWR# / GPIO0	P108	Camera 0 power enable, active low output	I/O 1.8V	PU 4k99	
CAM0_RST# / GPIO2	P110	Camera 0 reset, active low output	I/O 1.8V	PD(i) 20k	
I2C_CAM0_CK / CSI0_TX+	S5	I2C clock (serial camera support link for serial cameras).	I/O OD 1.8V	PU 1k58	Pull-up is active only during runtime
I2C_CAM0_DAT / CSI0_TX-	S7	I2C data (serial camera support link for serial cameras)	I/O OD 1.8V	PU 1k58	Pull-up is active only during runtime
CSI1_RX0+ CSI1_RX0-	P7 P8	CSI1 differential data pair 0	I LVDS D-PHY		

Signal	Pin #	Description	I/O	PU/PD	Comment
CSI1_RX1+ CSI1_RX1-	P10 P11	CSI1 differential data pair 1	I LVDS D-PHY		
CSI1_RX2+ CSI1_RX2-	P13 P14	CSI1 differential data pair 2	I LVDS D-PHY		
CSI1_Rx3+ CSI1_RX3-	P16 P17	CSI1 differential data pair 3	I LVDS D-PHY		
CSI1_CK+ CSI1_CK-	P3 P4	CSI1 differential clock pair	I LVDS D-PHY		
CAM1_PWR# / GPIO1	P109	Camera 1 power enable, active low output	I/O 1.8V	PU 4k99	
CAM1_RST# / GPIO3	P111	Camera 1 reset, active low output	I/O 1.8V	PD(i) 20k	
CAM_MCK	S6	Master clock output for CSI camera support. May be used for CSI0 or CSI1 or both	O 1.8V		
I2C_CAM1_CK / CSI1_TX+	S1	I2C clock (serial camera support link for serial cameras)	I/O OD 1.8V	PU 1k58	Pull-up is active only during runtime
I2C_CAM1_DAT / CSI1_TX-	S2	I2C data (serial camera support link for serial cameras)	I/O OD 1.8V	PU 1k58	Pull-up is active only during runtime

Table 18 SDIO Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SDIO_D0 SDIO_D1 SDIO_D2 SDIO_D3	P39 P40 P41 P42	SDIO Data lines	I/O 3.3V	PU(i) 20k	The SoC enables or disables the pull-up automatically depending on the transfer mode
SDIO_CMD	P34	SDIO Command/Response. This signal is used for card initialization and for command transfers	I/O 3.3V	PU(i) 20k	The SoC enables or disables the pull-up automatically depending on the transfer mode
SDIO_CK	P36	SDIO Clock. With each cycle of this signal a one-bit transfer on the command and each data line occurs	O 3.3V		
SDIO_WP	P33	SDIO Write Protect. This signal denotes the state of the write-protect tab on SD cards	I OD 3.3V	PU 10k	
SDIO_CD#	P35	SDIO Card Detect. This signal indicates when a SDIO/MMC card is present	I OD 3.3V	PU 10k	
SDIO_PWR_EN	P37	SDIO Power Enable. This signal is used to enable the power being supplied to a SD/MMC card device	O 3.3V		

Table 19 SPI0 Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SPI0_CS0#	P43	SPI0 master chip select 0 output for selecting SPI boot device	O 1.8V	PU 100k	Only for a BIOS flash device
SPI0_CS1#	P31	SPI0 master chip select output for selecting the second chip select when two devices are used. Do not use when only one SPI device is used	O 1.8V		Only for an SPI TPM device
SPI0_CK	P44	SPI0 master clock output	O 1.8V		
SPI0_DIN	P45	SPI0 master data input (SPI serial input data from the SPI device to SMARC® module)	I 1.8V		
SPI0_DO	P46	SPI0 master data output (SPI serial output data from SMARC® module to the SPI device	O 1.8V		

Note

1. *The conga-SA5 supports BIOS SPI flash memory and SPI TPM device on the SPI0 bus.*

2. *A custom BIOS is required for SPI TPM support.*

Table 20 eSPI/SPI1 Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
ESPI_CK	P56	ESPI master clock output. This pin provides the reference timing for all the serial input and output operations	O 1.8V	PD(i) 20k	
ESPI_CS0#	P54	ESPI master chip selet outputs. Driving Chip Select# low selects a particular eSPI slave for the transaction. Each of the eSPI slaves is connected to a dedicated Chip Select# pin	O 1.8V	PU 20k 1.8V	Only ESPI_CS0# supported
ESPI_CS1#	P55			PU 100k	
ESPI_IO_0	P58	ESPI master data input/outputs. These bi-directional input/output pins are used to transfer data between master and slaves. In single I/O mode, ESPI_IO_0 is the eSPI master output/eSPI slave input (MOSI) whereas ESPI_IO_1 is the eSPI master input/eSPI slave output (MISO)	I/O 1.8V	PD 2k49	ESPI_IO_2 and ESPI_IO_3 are not supported
ESPI_IO_1	P57			PU(i) 20k 1.8V	
ESPI_IO_2	S56			PU 100k 1.8V	
ESPI_IO_3	S57			PU 100k 1.8V	
ESPI_RESET#	S58	Resets the eSPI interface for both master and slaves. ESPI_RESET# is typically driven from eSPI master to eSPI slaves	O 1.8V	PU 100k 1.8V	Not supported
ESPI_ALERT0# ESPI_ALERT1#	S43 S44	This pin is used by eSPI slave to request service from eSPI master. Alert# is an open-drain output from the slave. This pin is optional for single master-single slave configuration where I/O[1] can be used to signal the alert event	I 1.8V	PU 100k 1.8V	Not supported

Note

The conga-SA5 supports only general purpose devices on the eSPI/SPI1 bus.

Table 21 I2S Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
I2S0_LRCK [1]	S39	Left and right audio synchronization clock	I/O 1.8V		Not connected
I2S0_SDOUT [1]	S40	Digital audio output	O 1.8V	PD 2K49	
I2S0_SDIN [1]	S41	Ditial audio input	I 1.8V		
I2S0_CK [1]	S42	Digital audio clock	I/O 1.8V		
AUDIO_MCK	S38	Master clock output to audio codecs	O 1.8V		

Note

1. *The I2S signals are not connected on the conga-SA5.*

Table 22 HDA Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
HDA_SYNC	S50	HD audio serial bus synchronization.	I/O 1.8V		
HDA_SDO	S51	HD audio serial data output to codec	O 1.8V		
HDA_SDI	S52	HD audio serial data input from codec	I 1.8V		
HDA_CK	S53	HD audio serial bit clock to codec	I/O 1.8V		
HDA_RST# / GPIO4	P112	HD audio codec reset	O 1.8V	PU 10k 1.8V	Pull-up is active only during runtime

Table 23 I2C Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
I2C_GP_CK	S48	I2C General purpose clock signal	I/O 1.8V	PU 1k	
I2C_GP_DAT	S49	I2C General purpose data signal	I/O 1.8V	PU 1k	

Table 24 Asynchronous Serial Port Signal Description

Signal	Pin #	Description	I/O	PU/PD	Comment
SER0_TX	P129	Asynchronous serial data output port 0	O 1.8V	PU 20k 1.8V	SoC UART: 1. Fully functional under Linux 2. Validated Intel HSUART driver for Windows 10 is available on the congatec website
SER0_RX	P130	Asynchronous serial data input port 0	I 1.8V	PU 20k 1.8V	
SER0_RTS#	P131	Request to Send handshake line for SER0	O 1.8V	PU 20k 1.8V	
SER0_CTS#	P132	Clear to Send handshake line for SER0	I 1.8V	PU 20k 1.8V	
SER1_TX	P134	Asynchronous serial data output port 1	O 1.8V		congatec Board Controller UART
SER1_RX	P135	Asynchronous serial data input port 1	I 1.8V		
SER2_TX	P136	Asynchronous serial data output port 2	O 1.8V	PU 20k 1.8V	SoC UART: 1. Fully functional under Linux 2. Validated Intel HSUART driver for Windows 10 is available on the congatec website
SER2_RX	P137	Asynchronous serial data input port 2	I 1.8V	PU 20k 1.8V	
SER2_RTS#	P138	Request to Send handshake line for SER2	O 1.8V	PU 20k 1.8V	
SER2_CTS#	P139	Clear to Send handshake line for SER2	I 1.8V	PU 20k 1.8V	
SER3_TX	P140	Asynchronous serial data output port 3	O 1.8V		congatec Board Controller UART
SER3_RX	P141	Asynchronous serial data input port 3	I 1.8V		

Table 25 USB Pinout Description

Signal	Pin #	Description	I/O	PU/PD	Comment
USB0+ USB0-	P60 P61	Differential USB 2.0 data pairs	I/O USB		
USB1+ USB1-	P65 P66	Differential USB 2.0 data pairs	I/O USB		
USB2+ USB2-	P69 P70	Differential USB 2.0 data pairs	I/O USB		
USB3+ USB3-	S68 S69	Differential USB 2.0 data pairs	I/O USB		
USB4+ USB4-	S35 S36	Differential USB 2.0 data pairs	I/O USB		
USB5+ USB5-	S59 S60	Differential USB 2.0 data pairs	I/O USB		
USB0_EN_OC# USB1_EN_OC# USB2_EN_OC# USB3_EN_OC# USB4_EN_OC# USB5_EN_OC#	P62 P67 P71 P74 P76 S55	Pulled low by module to disable USB0 power. Pulled low by carrier OD driver to indicate over-current situation. A pull-up to a 3.3V rail shall be present on the module	I/O OD 3.3V	PU 10k	PD 200k if USB port is not in use

USB0_VBUS_DET	P63	USB host power detection when this port is used as a device	I USB VBUS 5V	PD 1M	
USB3_VBUS_DET	S37	USB host power detection when this port is used as a device	I USB VBUS 5V		Not supported by default (assembly option)
USB0_OTG_ID USB3_OTG_ID	P64 S104	USB OTG ID input, active high	I 3.3V		Not supported
USB2SSRX+ USB2SSRX-	S74 S75	Receive signal differential pairs for SuperSpeed USB data coupling caps for RX pairs are off-module	I USB SS		
USB2SSTX+ USB2SSTX-	S71 S72	Transmit signal differential pairs for SuperSpeed USB data coupling caps for TX pairs are on-module	O USB SS		
USB3SSRX+ USB3SSRX-	S65 S66	Receive signal differential pairs for SuperSpeed USB data coupling caps for RX pairs are off-module	I USB SS		
USB3SSTX+ USB3SSTX-	S62 S63	Transmit signal differential pairs for SuperSpeed USB data coupling caps for TX pairs are on-module	O USB SS		

Note

1. *The conga-SA5 does not support USB OTG.*
2. *USB port 0 supports only USB 2.0 dual role.*
3. *USB port 3 supports USB 3.0 dual role only via assembly option.*

Table 26 PCIe Signal Description

Signal Name	Pin	Description	I/O	PU/PD	Comment
PCIE_A_TX+ PCIE_A_TX-	P89 P90	Differential PCIe link A transmit data pair	O LVDS PCIe		AC coupled with 100nF on module
PCIE_B_TX+ PCIE_B_TX-	S90 S91	Differential PCIe link B transmit data pair	O LVDS PCIe		AC coupled with 100nF on module
PCIE_C_TX+ PCIE_C_TX-	S81 S82	Differential PCIe link C transmit data pair	O LVDS PCIe		AC coupled with 100nF on module
PCIE_D_TX+ PCIE_D_TX-	S29 S30	Differential PCIe link D transmit data pair	O LVDS PCIe		AC coupled with 100nF on module
PCIE_A_RX+ PCIE_A_RX-	P86 P87	Differential PCIe link A receive data pair	I LVDS PCIe		
PCIE_B_RX+ PCIE_B_RX-	S87 S88	Differential PCIe link B receive data pair	I LVDS PCIe		
PCIE_C_RX+ PCIE_C_RX-	S78 S79	Differential PCIe link C receive data pair	I LVDS PCIe		

PCIE_D_RX+ PCIE_D_RX-	S32 S33	Differential PCIe link D receive data pair	I LVDS PCIe		
PCIE_A_REFCK+ PCIE_A_REFCK-	P83 P84	Differential PCIe Link reference clock output DC coupled	O LVDS PCIe		
PCIE_B_REFCK+ PCIE_B_REFCK-	S84 S85	Differential PCIe Link reference clock output DC coupled	O LVDS PCIe		
PCIE_C_REFCK+ PCIE_C_REFCK-	P80 P81	Differential PCIe Link reference clock output DC coupled	O LVDS PCIe		
PCIE_A_RST#	P75	PCIe port reset output	O 3.3V		
PCIE_B_RST#	S76	PCIe port reset output	O 3.3V		
PCIE_C_RST#	S77	PCIe port reset output	O 3.3V		
PCIE_WAKE#	S146	PCIe wake up interrupt to host common to PCIe links A, B, C, D	I OD 3.3V	PU 10k	

Table 27 SATA Signal Description

Signal Name	Pin	Description	I/O	PU/PD	Comment
SATA_TX+ SATA_TX-	P48 P49	SATA 0 transmit differential data pair	O SATA		Supports SATA specification, Revision 3.0
SATA_RX+ SATA_RX-	P51 P52	SATA 0 receive differential data pair	I SATA		Supports SATA specification, Revision 3.0
SATA_ACT#	S54	Active low SATA activity indicator	O OD 3.3V		Up to 24 mA

Table 28 Gigabit Ethernet Signal Description

Signal Name	Pin	Description	I/O	PU/PD	Comment
GBE0_MDI0+ GBE0_MDI0-	P30 P29	Bidirectional transmit/receive pair 0 to magnetics (Media Dependent Interface)	I/O GBE MDI		
GBE1_MDI0+ GBE1_MDI0-	S17 S18	Bidirectional transmit/receive pair 0 to magnetics (Media Dependent Interface)	I/O GBE MDI		
GBE0_MDI1+ GBE0_MDI1-	P27 P26	Bidirectional transmit/receive pair 1 to magnetics (Media Dependent Interface)	I/O GBE MDI		
GBE1_MDI1+ GBE1_MDI1-	S20 S21	Bidirectional transmit/receive pair 1 to magnetics (Media Dependent Interface)	I/O GBE MDI		
GBE0_MDI2+ GBE0_MDI2-	P24 P23	Bidirectional transmit/receive pair 2 to magnetics (Media Dependent Interface)	I/O GBE MDI		
GBE1_MDI2+ GBE1_MDI2-	S23 S24	Bidirectional transmit/receive pair 2 to magnetics (Media Dependent Interface)	I/O GBE MDI		
GBE0_MDI3+ GBE0_MDI3-	P20 P19	Bidirectional transmit/receive pair 3 to magnetics (Media Dependent Interface)	I/O GBE MDI		
GBE1_MDI3+ GBE1_MDI3-	S26 S27	Bidirectional transmit/receive pair 3 to magnetics (Media Dependent Interface)	I/O GBE MDI		
GBE0_LINK100# GBE1_LINK100#	P21 S19	Link speed indication LED for 100 Mbps	O OD 3.3V		Up to 24 mA
GBE0_LINK1000# GBE1_LINK1000#	P22 S22	Link speed indication LED for 1000 Mbps	O OD 3.3V		Up to 24 mA
GBE0_LINK_ACT# GBE1_LINK_ACT#	P25 S31	Link or activity indication LED. Driven low on link (10, 100 or 1000 Mbps). Blinks on Activity	O OD 3.3V		Up to 24 mA
GBE0_CTREF GBE1_CTREF	P28 S28	Center-Tap reference voltage for carrier board Ethernet magnetic (if required by the module GBE PHY)	O		Not connected
GBE0_SDP GBE1_SDP	P6 P5	IEEE 1588 trigger signal. For hardware implementation of PTP (precision time protocol). This is typically implemented by the software-defined pins from the Ethernet controller. The SDP pins can be used for IEEE1588 auxiliary device connections and for other miscellaneous hardware or software-control purposes	I/O 3.3V		Connected to onboard I210/I211 Ethernet controller pin SDP0

Table 29 Watchdog Signal Description

Signal Name	Pin	Description	I/O	PU/PD	Comment
WDT_TIME_OUT#	S145	Watchdog timer output	O 1.8V		Driven only during runtime

Table 30 GPIO Signal Description

Signal Name	Pin	Description	I/O	PU/PD	Comment
GPIO0 / CAM0_PWR#	P108	General purpose output 0 Alternate use: Camera 0 power enable CAM0_PWR# (active low output)	I/O 1.8V	PU 4k99	CAM0_PWR# is the default pin configuration. Pin is controlled by the SoC.
GPIO1 / CAM1_PWR#	P109	General purpose output 1 Alternate use: Camera 1 power enable CAM1_PWR# (active low output)	I/O 1.8V	PU 4k99	CAM1_PWR# is the default pin configuration. Pin is controlled by the SoC.
GPIO2 / CAM0_RST#	P110	General purpose output 2 Alternate use: Camera 0 reset CAM0_RST# (active low output)	I/O 1.8V	PD 20k	CAM0_RST# is the default pin configuration. Pin is controlled by the SoC.
GPIO3 / CAM1_RST#	P111	General purpose output 3 Alternate use: Camera 1 reset CAM1_RST# (active low output)	I/O 1.8V	PD 20k	CAM1_RST# is the default pin configuration. Pin is controlled by the SoC.
GPIO4 / HDA_RST#	P112	Bidirectional general purpose input/output 4, preferred for data output Alternate use: HD audio reset HDA_RST# (active low output)	I/O 1.8V	PU(i) 10k	HDA_RST# is the default pin configuration. Pin is controlled by the cBC.
GPIO5 / PWM_OUT	P113	Bidirectional general purpose input/output 5, preferred for data output Alternate use: Pulse Width Modulation output PWM_OUT	I/O 1.8V	PU(i) 10k	PWM_OUT is the default pin configuration. Pin is controlled by the cBC.
GPIO6 / TACHIN	P114	Bidirectional general purpose input/output 6, preferred for data input Alternate use: Tachometer input TACHIN	I/O 1.8V	PU(i) 10k	TACHIN is the default pin configuration Pin is controlled by the cBC.
GPIO7	P115	Bidirectional general purpose input/output 7	I/O 1.8V	PU 10k	Non-multiplexed GPIOs controlled by the cBC
GPIO8	P116	Bidirectional general purpose input/output 8	I/O 1.8V	PU 10k	
GPIO9	P117	Bidirectional general purpose input/output 9	I/O 1.8V	PU 10k	
GPIO10	P118	Bidirectional general purpose input/output 10	I/O 1.8V	PU 10k	
GPIO11	P119	Bidirectional general purpose input/output 11	I/O 1.8V	PU 10k	

Note

Pins P108-P114 do not support GPIO functionality by default. For GPIO functionality on these pins, change the default configuration in the BIOS menu under Advanced ->GPIO Configuration submenu.

Table 31 Management Pins Signal Description

Signal Name	Pin	Description	I/O	PU/PD	Comment
VIN_PWR_BAD#	S150	Power bad indication from carrier board. Module and carrier power supplies (other than module and carrier power supervisory circuits) will not be enabled while this signal is held low by the carrier. Pulled up on module. Driven by OD part on carrier	I VDD_IN	PU 22k6	
CARRIER_PWR_ ON	S154	Carrier board circuits (apart from power management and power path circuits) should not be powered up until the module asserts the CARRIER_PWR_ON signal.	O 1.8V		Connected to SUS_S4# signal
CARRIER_STBY#	S153	The module shall drive this signal low when the system is in a standby power state	O 1.8V		Connected to SUS_S3#
RESET_OUT#	P126	General purpose reset output to carrier board	O 1.8V		
RESET_IN#	P127	Reset input from carrier board. Carrier drives low to force a module reset, floats the line otherwise. Pulled up on module. Driven by OD part on carrier Note: For proper detection, assert a pulse width of at least 16 ms	I OD 3.3V	PU 20k	
POWER_BTN#	P128	Power-button input from carrier board. Carrier to float the line in in-active state. Active low, level sensitive. Should be de-bounced on the module. Pulled-up on module. Driven by OD part on carrier Note: For proper detection, assert a pulse width of at least 16 ms	I OD 3.3V	PU 10k	
SLEEP#	S149	Sleep indicator from carrier board. May be sourced from user Sleep button or carrier logic. Carrier to float the line in in-active state. Active low, level sensitive. Should be de-bounced on the module. Pulled-up on module. Driven by OD part on carrier Note: For proper detection, assert a pulse width of at least 16 ms	I OD 3.3V	PU 10k	
LID#	S148	Lid open/close indication to module. Low indicates lid closure (which system may use to initiate a sleep state). Carrier to float the line in in-active state. Active low, level sensitive. Should be de-bounced on the module. Pulled-up on module. Driven by OD part on carrier Note: For proper detection, assert a pulse width of at least 16 ms	I OD 3.3V	PU 10k	
BATLOW#	S156	Battery low indication to module. Carrier to float the line in in-active state. Pulled up on module. Driven by OD part on carrier	I OD 1.8V	PU 10k	
I2C_PM_DAT I2C_PM_CK	P122 P121	Power management I2C bus data and clock. On x86 systems these serve as SMB data and clock	I/O OD 1.8V	PU 1k	
CHARGING#	S151	Held low by carrier during battery charging. Carrier to float the line when charge is complete. Pulled-up on module. Driven by OD part on carrier	I OD 3.3V	PU 10k 3.3V	
CHARGER_ PRSNT#	S152	Held low by carrier if DC input for battery charger is present. Pulled up on module. Driven by OD part on carrier	I OD 3.3V	PU 10k 3.3V	
TEST#	S157	Held low by carrier to invoke module vendor specific test function(s). Pulled up on module. Driven by OD part on carrier	I OD 3.3V	PU 100k 3.3V	
SMB_ALERT_1V8#	P1	SM Bus Alert# (interrupt) signal	I OD 1.8V	PU 1k7	

Table 32 Boot Select Signal Description

Signal Name	Pin	Description	I/O	PU/PD	Comment
BOOT_SEL0# BOOT_SEL1# BOOT_SEL2#	P123 P124 P125	Input straps determine the module boot device. Pulled up on module. Driven by OD part on carrier	I 1.8V	PU 10k	
FORCE_RECOV#	S155	Low on this pin allows non-protected segments of module boot device to be rewritten or restored from an external USB Host on module USB0. The module USB0 operates in Client Mode when the Force Recovery function is invoked. Pulled high on the module. For SoCs that do not implement a USB based Force Recovery functions, then a low on the module FORCE_RECOV# pin may invoke the SOC native Force Recovery mode – such as over a Serial Port. For x86 systems this signal may be used to load BIOS defaults. Pulled up on module. Driven by OD part on carrier	I 1.8V	PU 20k	Not supported

Table 32.1 Boot Source Description

Carrier Connection			Boot Source
BOOT_SEL2#	BOOT_SEL1#	BOOT_SEL0#	
GND	GND	GND	Carrier SATA
GND	GND	Float	Carrier SD Card
GND	Float	GND	Carrier eSPI (CS0#)
GND	Float	Float	Carrier SPI (CS0#)
Float	GND	GND	Module device (NAND, NOR) - vendor specific
Float	GND	Float	Remote boot (GbE, serial) - vendor specific
Float	Float	GND	Module eMMC flash
Float	Float	Float	Module SPI

Note

The conga-SA5 supports only Carrier SPI boot source configuration (GND, Float, Float) . With this configuration, the conga-SA5 will load the UEFI firmware from carrier board SPI device. For other boot source configurations, the conga-SA5 will load the UEFI firmware from on-module SPI flash.

Table 32.2 Boot Strap Signal Description

Signal	Pin #	Description of Boot Strap Signal	I/O	PU/PD	Comment
ESPI_CS0#	P54	ESPI master chip select output 0	O 1.8V	PD 20k	
ESPI_CS1#	P55	ESPI master chip select output 0	O 1.8V	PU 20k	
ESPI_CK	P56	ESPI master clock output	O 1.8V	PD 20k	
SER0_TX	P129	Asynchronous serial port 0 data out	O 1.8V	PD 20k	
SER0_RTS#	P131	Request to Send handshake for serial port 0	O 1.8V	PD 20k	
SER2_TX	P136	Asynchronous serial port 2 data out	O 1.8V	PD 2K49	
SER2_RTS#	P138	Request to Send handshake for serial port 2	O 1.8V	PU 20k	
ESPI_IO_0	P58	ESPI master data input/output	O 1.8V	PD 2k49	

Caution

1. *The signals listed in the table above are used as chipset configuration straps during system reset. In this condition (during reset), they are inputs that are pulled to the correct state by either SMARC internally implemented resistors or chipset internally implemented resistors that are located on the module.*

2. *No external DC loads or external pull-up or pull-down resistors should change the configuration of the signals listed in the above table.*

3. *External resistors may override the internal strap states and cause the SMARC module to malfunction and/or cause irreparable damage to the module.*

Table 33 Power and GND Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
VDD_IN	P147, P148, P149, P150, P151, P152, P153, P154, P155, P156	Module power input voltage—4.75V min. to 5.25V max.	P		
GND	P2, P9, P12, P15, P18, P32, P38, P47, P50, P53, P59, P68, P79, P82, P85, P88, P91, P94, P97, P100, P103, P120, P133, P142 S3, S10, S16, S25, S34, S47, S61, S64, S67, S70, S73, S80, S83, S86, S89, S92, S101, S110, S119, S124, S130, S136, S143, S158	Power Ground	P		
VDD_RTC	S147	Low current RTC circuit backup power—3.0V nominal. May be sourced from a carrier based lithium cell or super cap. This option requires a customized variant.	P		BOM option for sourcing

Note

External 3.3 V is required for RTC battery implementation with supercap. Default conga-SA5 configuration does not support supercap charging. The supercap charging is only possible with a BOM option.

9 System Resources

9.1 I/O Address Assignment

The I/O address assignment of the conga-SA5 module is functionally identical with a standard PC/AT. The table below shows the most important addresses and the addresses that differ from the standard PC/AT configuration.

Table 34 I/O Address Assignment

I/O Address (hex)	Size	Available	Description
0000 - 00FF	256 bytes	No	Motherboard resources
03B0 - 03CF	32 bytes	No	Video system
0400 - 047F	128 bytes	No	Motherboard resources
0500 - 05FF	256 bytes	No	Motherboard resources
0680 - 069F	20 bytes	No	Motherboard resources
0CF8 - 0CFB	4 bytes	No	PCI configuration address register
0CFC - 0CFF	4 bytes	No	PCI configuration data register
0D00 - F000		See note	PCI / PCI Express bus

Note

1. *The BIOS assigns PCI and PCI Express I/O resources from F000h downwards.*

2. *Devices that are not compliant to PnP, PCI or PCI Express must not use any I/O resource in this address range.*

9.2 PCI Configuration Space Map

Table 35 PCI Configuration Space Map

Bus Number (hex)	Device Number (hex)	Function Number (hex)	Device ID	Description and Device ID
00h	00h	00h	0x5AF0	Host Bridge
00h	02h	00h	0x5A84	Graphics and Display
00h	0Dh	00h	0x5A92	Primary to SideBand Bridge
00h	0Dh	01h	0x5A94	PMC (Power Management Controller)
00h	0Dh	02h	0x5A96	Fast SPI
00h	0Dh	03h	0x5AEC	Shared SRAM
00h	0Eh	00h	0x5A98	HDA
00h	0Fh	00h	0x5A9A	Simple Communication Controller 0
00h	0Fh	01h	0x5A9C	Simple Communication Controller 1
00h	0Fh	02h	0x5A9E	Simple Communication Controller 2
00h	012h	00h	0x5AE3	SATA
00h	013h	00h	0x5AD8	PCIe - A0
00h	013h	01h	0x5AD9	PCIe - A1 [1]
00h	013h	02h	0x5ADA	PCIe - A2 [1]
00h	013h	03h	0x5ADB	PCIe - A3 [1]
00h	014h	00h	0x5AD6	PCIe -B0
00h	015h	00h	0x5AA8	USB-Host (xHCI)
00h	015h	01h	0x5AAA	USB-Host (xDCI)
00h	016h	00h	0x5AAC	I2C 0 [2]
00h	016h	01h	0x5AAE	I2C 1 [2]
00h	016h	02h	0x5AB0	I2C 2 [2]
00h	016h	03h	0x5AB2	I2C 3 [2]
00h	017h	00h	0x5AB4	I2C 4 [2]
00h	017h	00h	0x5AB6	I2C 5 [2]
00h	017h	00h	0x5AB8	I2C 6 [2]
00h	017h	00h	0x5ABA	I2C 7 [2]
00h	018h	00h	0x5ABC	SoC UART 0 [2]
00h	018h	01h	0x5ABE	SoC UART 1 [2]
00h	018h	02h	0x5AC0	SoC UART 2 [2]
00h	018h	03h	0x5AEE	SoC UART 3 [2]

00h	019h	00h	0x5AC2	SPI 0 [2]
00h	019h	01h	0x5AC4	SPI 1 [2]
00h	019h	02h	0x5AC6	SPI 2 [2]
00h	01Bh	00h	0x5ACA	SD Card
00h	01Ch	01h	0x5ACC	eMMC
00h	01Fh	00h	0x5AE8	LPC Bus
00h	01Fh	01h	0x5AD4	SM Bus
02h	00h	00h	0x1539	Intel® PCIe Ethernet Network on module

Note

1. *To view these ports, attach a device to the corresponding PCI Express port or set the PCI Express port in the BIOS setup menu to "Enabled".*
2. *Disabled by default in the BIOS Setup menu.*

9.3 I²C Bus and SMBus

The table below describes the use and access of several buses on the conga-SA5.

Table 36 Bus Accessibility

Bus Unit	Bus Number	Bus Type Identifier	Bus Type	Use
0	0	00010000	I2C	User accessible bus—no onboard resource is connected to the I²C bus. Address 16h is reserved for congatec battery management solutions.
1	2	00020000	SMBus	SMBus signals are connected to Intel® Apollo Lake Soc. Therefore, do not use for off-board non-system management devices.
2	4	00030000	EPI	EPI Panel Bus
3	3	00040000	Virtual Bus	Do not use
4	1	00020000	SMBus	Do not use
5	5	00050000	Aux Bus	Do not use

10 BIOS Setup Description

The BIOS setup description of the conga-SA5 can be viewed without having access to the module. However, access to the restricted area of the congatec website is required in order to download the necessary tool (CgMlfViewer) and Menu Layout File (MLF).

The MLF contains the BIOS setup description of a particular BIOS revision. The MLF can be viewed with the CgMlfViewer tool. This tool offers a search function to quickly check for supported BIOS features. It also shows where each feature can be found in the BIOS setup menu.

For more information, read the application note "AN42 - BIOS Setup Description" available at www.congatec.com.

Note

If you do not have access to the restricted area of the congatec website, contact your local congatec sales representative.

10.1 Navigating the BIOS Setup Menu

The BIOS setup menu shows the features and options supported in the congatec BIOS. To access and navigate the BIOS setup menu, press the <DEL> or <F2> key during POST. The right frame displays the key legend. Above the key legend is an area reserved for text messages. These text messages explain the options and the possible impacts when changing the selected option in the left frame.

10.2 BIOS Versions

The BIOS displays the BIOS project name and the revision code during POST, and on the main setup screen. The initial production BIOS for conga-SA5 is identified as SA50R1xx, where:

- R is the identifier for a BIOS ROM file,
- 1 is the so called feature number and
- xx is the major and minor revision number.

The SA50 binary size is 8 MB.

10.3 Updating the BIOS

BIOS updates are recommended to correct platform issues or enhance the feature set of the module. The conga-SA5 features a congatec/AMI AptioEFI firmware on an onboard flash ROM chip. You can update the firmware with the congatec System Utility. The utility has five versions—UEFI shell, DOS based command line[1], Win32 command line, Win32 GUI, and Linux version.

For more information about "Updating the BIOS" refer to the user's guide for the congatec System Utility "CGUTLm1x.pdf" on the congatec website at www.congatec.com.

Note

1. *Deprecated*

Caution

The DOS command line tool is not officially supported by congatec and therefore not recommended for critical tasks such as firmware updates. We recommend to use only the UEFI shell for critical updates.

10.3.1 Update from External Flash

For instructions on how to update the BIOS from external flash, refer to the AN7_External_BIOS_Update.pdf application note on the congatec website at http://www.congatec.com.

10.4 Supported Flash Devices

The conga-SA5 supports the following flash devices:

- Winbond W25Q64FWSSIQ (8 MB)
- Macronix MX25U6473FM2I-10G (8 MB)
- GigaDevice GD25LB64CSIG (8 MB)

The flash devices listed above can be used on the carrier board to support external BIOS.