APRO Co., Ltd.

SLC

Industrial Micro IDE Flash Module

HERMIT-A Series

Document No. : 100-xxMIF-HATL

Version No. : 02V0

Date : June, 2019

ISO 9001 : 2015 CERTIFIED

Product Features

- **Flash IC**
  - TOSHIBA NAND Flash IC.
  - Single-Level Cell (SLC) management technology.

- **Compatibility**
  - ATA-6 standard compatible in True-IDE mode.

- **Additional Capabilities**
  - Fast ATA host-to-buffer transfer rates supporting PIO mode 6, MDMA mode 2, UDMA mode 4 in True-IDE mode
  - S.M.A.R.T.[*1] (Self-Monitoring, Analysis and Reporting Technology) feature set support.
  - Static wear leveling algorithm
  - Support bad Block Management

- **Mechanical**
  - Standard 40-pin IDE connector consisting of two rows of 20 female contacts w/2.54mm pin-pitch.
  - Standard 44-pin IDE connector consisting of two rows of 22 female contacts w/2.00mm pin-pitch.
  - **Dimension:**
    40-pin Vertical: 60.20 mm x 27.79mm x 6.4mm
    40-pin Horizontal: 55.00 mm x 32.4mm
    44-pin Vertical: 50.25 mm x 27.27mm x 5.8mm
    44-pin Horizontal: 48.00 mm x 32.4mm
  - **Weight:**
    40-pin Vertical: 20g / 0.70 oz.
    40-pin Horizontal: 15g / 0.52 oz.
    44-pin Vertical: 15g / 0.52 oz.
    44-pin Horizontal: 12g / 0.42 oz.

- **Power: Operating Voltage @ 5V(+/-) 10%**
  - Read Mode: 178.0 mA (max.)
  - Write Mode: 142.5 mA (max.)
  - Idle Mode: 0.9 mA (max.)

- **Performance (Maximum value) *[2]**
  - Sequential Read: 39.5 MB/sec. (max.)
  - Sequential Write: 28.0 MB/sec. (max.)

- **Capacity**
  - Vertical Type capacity from 16MB to 4GB
  - Horizontal Type capacity from 16MB to 8GB

- **Reliability**
  - **TBW:** Up to 421.8 TBW at 8GB Capacity. (Test by sequential write)
  - **ECC:** 4-Bit per 512 bytes in an ECC block.
  - **MTBF:** > 3,000,000 hours
  - **Temperature:** (Operating)
    Standard Grade: 0ºC ~ +70ºC
    Industrial Grade: -40ºC ~ +85ºC
  - **Vibration:** 70 Hz to 2K Hz, 20G, 3 axes.
  - **Shock:** 0.5ms, 1500 G, 3 axes

- **Certifications and Declarations**
  - **Certifications**: CE & FCC
  - **Declarations**: RoHS & REACH

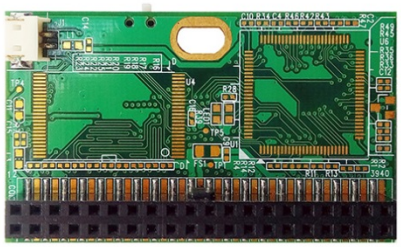
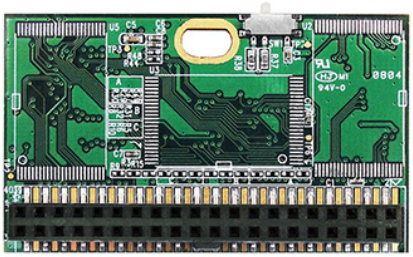
Remarks:

1. Support official S.M.A.R.T. Utility.
2. Sequential performance is based on CrystalDiskMark 5.1.2 with file size 100MB

Order Information

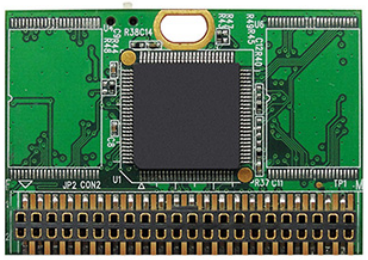
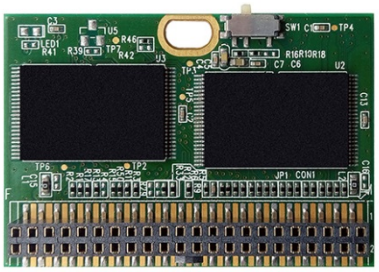
I. Part Number List

◆ **APRO SLC Industrial MIF HERMIT-A Series 40pin Vertical / Horizontal Rightward / Horizontal Leftward**

Product Picture		
40pin vertical type	40pin horizontal-rightward	40pin horizontal-leftward
		

Data transfer mode setting by PIO-4(P), UDMA-4(U) or auto detection (A)			
Capacity	Form-factor	STD. grade 0°C ~ 70°C	IND. grade -40°C ~ 85°C
16MB	Vertical	SPMIF016M-HACTC-0V(P)(U)(A)	WPMIF016M-HAITI-0V(P)(U)(A)
	Right	SBMIF016M-HACTC-0R(P)(U)(A)	WBMIF016M-HAITI-0R(P)(U)(A)
	Left	SBMIF016M-HACTC-0L(P)(U)(A)	WBMIF016M-HAITI-0L(P)(U)(A)
32MB	Vertical	SPMIF032M-HACTC-0V(P)(U)(A)	WPMIF032M-HAITI-0V(P)(U)(A)
	Right	SBMIF032M-HACTC-0R(P)(U)(A)	WBMIF032M-HAITI-0R(P)(U)(A)
	Left	SBMIF032M-HACTC-0L(P)(U)(A)	WBMIF032M-HAITI-0L(P)(U)(A)
64MB	Vertical	SPMIF064M-HACTC-0V(P)(U)(A)	WPMIF064M-HAITI-0V(P)(U)(A)
	Right	SBMIF064M-HACTC-0R(P)(U)(A)	WBMIF064M-HAITI-0R(P)(U)(A)
	Left	SBMIF064M-HACTC-0L(P)(U)(A)	WBMIF064M-HAITI-0L(P)(U)(A)
128MB	Vertical	SPMIF128M-HACTC-0V(P)(U)(A)	WPMIF128M-HAITI-0V(P)(U)(A)
	Right	SBMIF128M-HACTC-0R(P)(U)(A)	WBMIF128M-HAITI-0R(P)(U)(A)
	Left	SBMIF128M-HACTC-0L(P)(U)(A)	WBMIF128M-HAITI-0L(P)(U)(A)
256MB	Vertical	SPMIF256M-HACTC-0V(P)(U)(A)	WPMIF256M-HAITI-0V(P)(U)(A)
	Right	SBMIF256M-HACTC-0R(P)(U)(A)	WBMIF256M-HAITI-0R(P)(U)(A)
	Left	SBMIF256M-HACTC-0L(P)(U)(A)	WBMIF256M-HAITI-0L(P)(U)(A)
512MB	Vertical	SPMIF512M-HACTC-0V(P)(U)(A)	WPMIF512M-HAITI-0V(P)(U)(A)
	Right	SBMIF512M-HACTC-0R(P)(U)(A)	WBMIF512M-HAITI-0R(P)(U)(A)
	Left	SBMIF512M-HACTC-0L(P)(U)(A)	WBMIF512M-HAITI-0L(P)(U)(A)
1GB	Vertical	SPMIF001G-HACTC-0V(P)(U)(A)	WPMIF001G-HAITI-0V(P)(U)(A)
	Right	SBMIF001G -HACTC-0R(P)(U)(A)	WBMIF001G -HAITI-0R(P)(U)(A)
	Left	SBMIF001G -HACTC-0L(P)(U)(A)	WBMIF001G -HAITI-0L(P)(U)(A)
2GB	Vertical	SPMIF002G-HACTC-0V(P)(U)(A)	WPMIF002G-HAITI-0V(P)(U)(A)
	Right	SBMIF002G -HACTC-0R(P)(U)(A)	WBMIF002G -HAITI-0R(P)(U)(A)C
	Left	SBMIF002G -HACTC-0L(P)(U)(A)	WBMIF002G -HAITI-0L(P)(U)(A)C
4GB	Vertical	SPMIF004G-HACTC-0V(P)(U)(A)	WPMIF004G-HAITI-0V(P)(U)(A)C
	Right	SBMIF004G -HACTC-0R(P)(U)(A)	WBMIF004G -HAITI-0R(P)(U)(A)C
	Left	SBMIF004G -HACTC-0L(P)(U)(A)	WBMIF004G -HAITI-0L(P)(U)(A)C
8GB	Vertical	**Do not support**	**Do not support**
	Right	SBMIF008G -HACTC-0R(P)(U)(A)	WBMIF008G -HAITI-0R(P)(U)(A)
	Left	SBMIF008G -HACTC-0L(P)(U)(A)	WBMIF008G -HAITI-0L(P)(U)(A)

◆ **APRO SLC Industrial MIF HERMIT-A Series 44pin Vertical / Horizontal Rightward / Horizontal Leftward**

Product Picture		
44pin vertical type	44pin horizontal-rightward	44pin horizontal-leftward
		

Data transfer mode setting by PIO-4(P), UDMA-4(U) or auto detection (A)			
Capacity	Form-factor	STD. grade 0°C ~ 70°C	IND. grade -40°C ~ 85°C
16MB	Vertical	SPMIF016M-HACTC-4V(P)(U)(A)	WPMIF016M-HAITI-4V(P)(U)(A)
	Right	SBMIF016M-HACTC-4R(P)(U)(A)	WBMIF016M-HAITI-4R(P)(U)(A)
	Left	SBMIF016M-HACTC-4L(P)(U)(A)	WBMIF016M-HAITI-4L(P)(U)(A)
32MB	Vertical	SPMIF032M-HACTC-4V(P)(U)(A)	WPMIF032M-HAITI-4V(P)(U)(A)
	Right	SBMIF032M-HACTC-4R(P)(U)(A)	WBMIF032M-HAITI-4R(P)(U)(A)
	Left	SBMIF032M-HACTC-4L(P)(U)(A)	WBMIF032M-HAITI-4L(P)(U)(A)
64MB	Vertical	SPMIF064M-HACTC-4V(P)(U)(A)	WPMIF064M-HAITI-4V(P)(U)(A)
	Right	SBMIF064M-HACTC-4R(P)(U)(A)	WBMIF064M-HAITI-4R(P)(U)(A)
	Left	SBMIF064M-HACTC-4L(P)(U)(A)	WBMIF064M-HAITI-4L(P)(U)(A)
128MB	Vertical	SPMIF128M-HACTC-4V(P)(U)(A)	WPMIF128M-HAITI-4V(P)(U)(A)
	Right	SBMIF128M-HACTC-4R(P)(U)(A)	WBMIF128M-HAITI-4R(P)(U)(A)
	Left	SBMIF128M-HACTC-4L(P)(U)(A)	WBMIF128M-HAITI-4L(P)(U)(A)
256MB	Vertical	SPMIF256M-HACTC-4V(P)(U)(A)	WPMIF256M-HAITI-4V(P)(U)(A)
	Right	SBMIF256M-HACTC-4R(P)(U)(A)	WBMIF256M-HAITI-4R(P)(U)(A)
	Left	SBMIF256M-HACTC-4L(P)(U)(A)	WBMIF256M-HAITI-4L(P)(U)(A)
512MB	Vertical	SPMIF512M-HACTC-4V(P)(U)(A)	WPMIF512M-HAITI-4V(P)(U)(A)
	Right	SBMIF512M-HACTC-4R(P)(U)(A)	WBMIF512M-HAITI-4R(P)(U)(A)
	Left	SBMIF512M-HACTC-4L(P)(U)(A)	WBMIF512M-HAITI-4L(P)(U)(A)
1GB	Vertical	SPMIF001G-HACTC-4V(P)(U)(A)	WPMIF001G-HAITI-4V(P)(U)(A)
	Right	SBMIF001G-HACTC-4R(P)(U)(A)	WBMIF001G-HAITI-4R(P)(U)(A)
	Left	SBMIF001G-HACTC-4L(P)(U)(A)	WBMIF001G-HAITI-4L(P)(U)(A)
2GB	Vertical	SPMIF002G-HACTC-4V(P)(U)(A)	WPMIF002G-HAITI-4V(P)(U)(A)
	Right	SBMIF002G-HACTC-4R(P)(U)(A)	WBMIF002G-HAITI-4R(P)(U)(A)
	Left	SBMIF002G-HACTC-4L(P)(U)(A)	WBMIF002G-HAITI-4L(P)(U)(A)
4GB	Vertical	SPMIF004G-HACTC-4V(P)(U)(A)	WPMIF004G-HAITI-4V(P)(U)(A)
	Right	SBMIF004G-HACTC-4R(P)(U)(A)	WBMIF004G-HAITI-4R(P)(U)(A)
	Left	SBMIF004G-HACTC-4L(P)(U)(A)	WBMIF004G-HAITI-4L(P)(U)(A)
8GB	Vertical	**Do not support**	**Do not support**
	Right	SBMIF008G-HACTC-4R(P)(U)(A)	WBMIF008G-HAITI-4R(P)(U)(A)
	Left	SBMIF008G-HACTC-4L(P)(U)(A)	WBMIF008G-HAITI-4L(P)(U)(A)

II. Part Number Decoder:

X1 X2 X3 X4 X5 X6 X7 X8 X9 — X11 X12 X13 X14 X15 — X17 X18 X19 X20

X1 : **Grade**

S: Standard Grade – operating temp. 0º C ~ 70 º C

W: Industrial Grade- operating temp. -40º C ~ +85 º C

X2 : **The material of case**

B : Bare (without case)

P : Plastic case

X3 X4 X5 : **Product category**

MIF : micro IDE Flash (module)

X6 X7 X8 X9 : **Capacity**

16M:	16MB	**512M:**	512MB
32M:	32MB	**001G:**	1GB
64M:	64MB	**002G:**	2GB
128M:	128MB	**004G:**	4GB
256M:	256MB	**008G:**	8GB

X11 : **Controller**

H : HERMIT Series

X12 : **Controller version**

A, B, C.....

X13 : **Controller Grade**

C : Commercial grade

I : Industrial grade

X14 : **Flash IC**

T : Toshiba SLC NAND Flash IC

X15 : **Flash IC grade / Type**

C : Commercial grade

I : Industrial grade

X17 X18 : **MIF orient only**

0V : 40-pin IDE Vertical MIF

0R : 40-pin IDE Right-oriented MIF

0L : 40-pin IDE Left-oriented MIF

4V : 44-pin IDE Vertical MIF

4R : 44-pin IDE Right-oriented MIF

4L : 44-pin IDE Left-oriented MIF

X19 : **Data transfer rate**

IDE interface is always Fixed Disk Mode

P : PIO-6 mode

U : UDMA-4 mode (Def.)

A : Auto PIO or UDMA mode

X20 : **Reserved for specific requirement**

C : Conformal coating (optional)

Revision History

Revision	Description	Date
1.0	Initial release	2013/11/08
1.1	Updated Version	2018/11/28
2.0	Updated power consumption & performance	2019/05/16

Contents

1. Introduction

APRO SLC Industrial Micro IDE Flash (MIF) Module HERMIT-A Series complies with ATA-6 standard. The main used Flash memories are SLC-NAND Type Flash memory chips from 16MB up to 8GB. The operating temperature grade is optional for standard grade 0°C ~ 70°C and industrial grade -40°C ~ +85°C.

The APRO SLC Industrial Micro IDE Flash (MIF) Module HERMIT-A Series supports S.M.A.R.T. function and designed electrically compliant with the conventional IDE hard disk and support True IDE Mode. The data transfer modes supports PIO 0~4, Multi Word DMA 0~2, or UDMA 0~4; Default setting are PIO mode-4 or UDMA-4. HERMIT Series MIF features an extremely light weight, reliable, low-profile form factor.

The APRO SLC Industrial Micro IDE Flash (MIF) Module HERMIT-A Series provides a high level interface to the host computer. This interface allows a host computer to issue commands to the Flash Module to read or write blocks of memory. Each sector is protected by a powerful 4-Bit per 512 bytes in an ECC block. APRO SLC Industrial Micro IDE Flash (MIF) Module HERMIT-A Series uses intelligent controller which manages interface protocols, data storage and retrieval as well as ECC, defect handling and diagnostics, power management and clock control.

Figure 1 shows a block diagram of the used high tech APRO SLC Industrial Micro IDE Flash (MIF) Module HERMIT-A Series

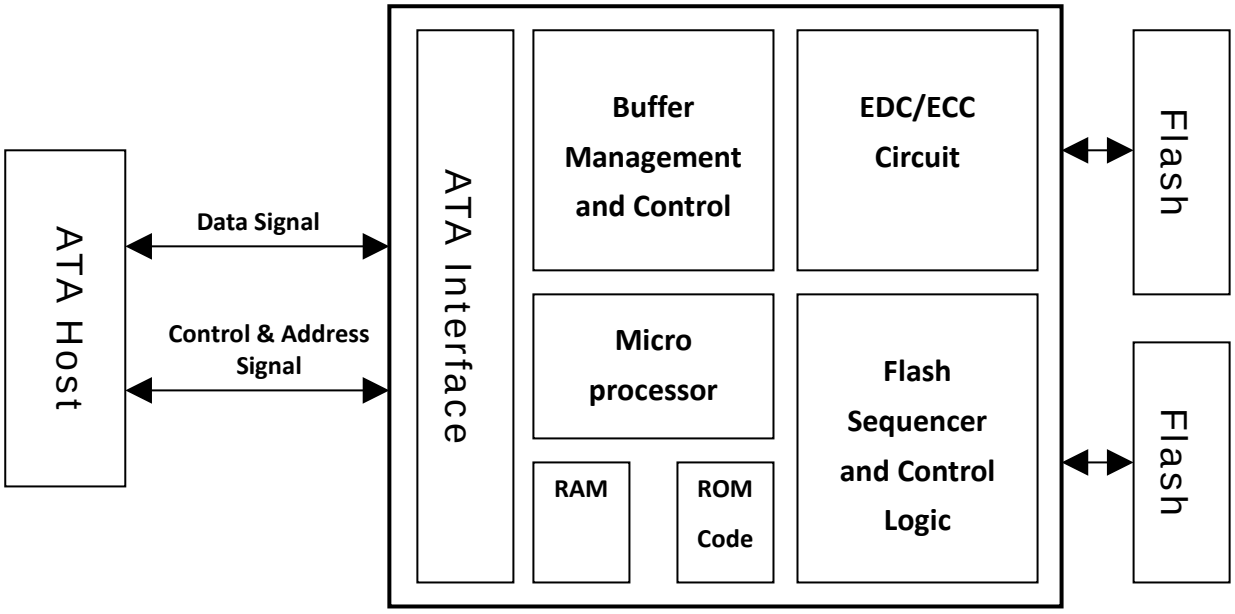


Figure 1: APRO SLC Industrial Micro IDE Flash Module HERMIT-A Series block diagram

1.1. *Scope*

This document describes features, specifications and installation guide of APRO SLC Industrial Micro IDE Flash (MIF) Module HERMIT-A Series. The appendix provides order information, warranty policy, RMA/DOA procedure for the most convenient reference.

1.2. *Flash Management Technology – Static Wear leveling*

In order to gain the best management for flash memory, APRO SLC Industrial Micro IDE Flash (MIF) Module HERMIT-A Series supports Static Wear Leveling technology to manage the Flash system. The life of flash memory is limited; the management is to increase the life of the flash product.

A static wear-leveling algorithm evenly distributes data over an entire Flash cell array and searches for the least used physical blocks. The identified low cycled sectors are used to write the data to those locations. If blocks are empty, the write occurs normally. If blocks contain static data, it moves that data to a more heavily used location before it moves the newly written data. The static wear leveling maximizes effective endurance Flash array compared to no wear leveling or dynamic wear leveling.

1.3. *Protected against data corruption and failing devices*

- **Sudden Power Fail (SPF) Event**
  - Reset of controller and immediate write protection of flash
  - If the last data written is corrupt, controller recovers latest valid entry
  - If a write operation is active at power loss this data might be lost
- **Transaction-oriented logging of mapping changes**
  - All mapping information is kept in non-volatile storage
  - SLC-aware Power Fail Management
  - Option: Reliable Write of user data
- **Rigorous Testing to ensure functionality**
  - Power Cycling Test
  - Stress Test
  - Regression Test

1.4. *Bad Block Management*

- **Early Bad Block**

The fault block generated during the manufacturing process of NAND Flash is called Early Bad Block.

- **Later Bad Block**

In the process of use, as the number of operations of writing and erasing increases, a fault block is gradually generated, which is called a Later Bad Block.

Bad block management is a management mechanism for a bad block to be detected by the control IC and mark bad blocks in the NAND Flash and improve the reliability of data access. The bad block management mechanism of the control IC will establish a **Bad Block Table** when the NAND Flash is started for the first time, and will also record the errors found in the process of use in the bad block table, and data is ported to new valid blocks to avoid data loss.

In order to detect the initial bad blocks to handle run time bad blocks, APRO SLC Industrial Micro IDE Flash (MIF) Module HERMIT-A Series provides the **Bad Block Management** scheme. It remaps a bad block to one of the reserved blocks so that the data contained in one bad block is not lost and new data writes on a bad block is avoided.

1.5. *Mean Time Between Failure (MTBF)*

1.5.1. Definition

MTBF (Mean time between failures) is defined as failure or maintenance required for the average time including failure detection and maintenance for the device. For a simple and maintainable unit, MTBF = MTTF + MTTR.

MTTF (mean time to failure) is defined as the expectation of random variables for time to failure.

MTTR（**mean time to restoration**） is the expectation of random variables of time required for restoration which includes the time required for confirmation that a failure occurred, as well as the time required for maintenance.

1.5.2. Obtaining MTBF

There are two methods for obtaining MTBF:

A. MTBF software estimation method: by calculating all the MTBF data of all the components included in the bill of material, and the data of the completed products including actual parameters of voltage and electrical current using analysis software, the MTBF of the completed product is estimated.

B. MTBF sample test method: by determining a certain number of samples and a fixed time for testing, using a Arrhenius Model and Coffin-Manson Model to obtain parameters, and then using the formula with the parameters, the longevity and in so the reliability is proved.

Arrhenius Model: $\mathbf{Af = e\{ (1/k \times Ea (1/273+Tmax - 1/273+Ttest)\}}$

Coffin-Manson Model: $\mathbf{Af = (\Delta Ttest/\Delta Tuse)m}$

- **APRO uses the A method to Estimate MTBF**

MTBF is actually obtained by calculation which is just an estimation of future occurrences. The main reason to use the first method is that the data contains the analysis by all the parameters of components and actual parameters of voltage and electrical current of finished products, which is considered adequate and objective.

➢ **Interpretation of MTBF Analysis**

APRO estimates MTBF using a prediction methodology based on reliability data for the individual components in APRO products. The predicted MTBF based on Parts stress analysis Method of Telcordia Special Report SR-332, for components failure rates. Component data comes from several sources: device life tests, failure analysis of earlier equipment, device physics, and field returns.

The Telcordia model is based on the Telcordia document, Reliability Prediction Procedure for Electronic Equipment, Technical Reference SR-332. This standard basically modified the component models in MIL-HDBK-217 to better reflect the failure rates that AT&T Bell Lab equipment was experiencing in the field and was originally developed by AT&T Bell Lab as the Bellcore model.

This model supports different failure rate calculation methods in order to support the taking into account of stress, burn-in, laboratory, or field data. A Parts Count or Parts Stress analysis is included in Telcordia performance. Relex supports Telcordia Issues 1 and 2 and also Bellcore Issues 4, 5, and 6.Telcordia Issue 2, released in September 2006, are supported by Relex and Telcordia Issue 1, released in May 2001, is replaced with Relex. Refer to Telcordia Issue 2 Fields for information about the fields in Relex Reliability Studio specific to Telcordia Issue 2.

➢ **Purpose of the analyses**

The purpose of these analyses is to obtain early estimation of device reliability during engineering and customer validation stages. The prediction results will expose the reliability of whole assembly, viewed as a set of serially connected electronic components. Rating of the assembly electronic components will show the ratio between actual critical elements parameters and their specification limits. The purpose of component rating is to improve a product's inherent design reliability, increase its number of operating times, and to reduce warranty costs and to achieve a more robust design.

1.5.3. Definitions

Term	Definition
Failure	The event, or inoperable state, in which any item or part of an item does not, or would not, perform as previously specified.
Failure rate	The total number of failures within an item population, divided by the total number of life units expended by that population, during a particular measurement interval under stated condition.
FIT	Failures In Time: the number of failures in 1 billion hours.
PPM	Part per million: the number of failures in 1 million hours.
Mean Time Between Failures (MTBF)	A basic measure of reliability for repairable items: The mean number of life units during which all parts of the item perform within their specified limits, during a particular measurement interval under stated conditions..
GB	Ground, Fixed, Controlled: Nearly zero environmental stress with optimum engineering operation and maintenance. Typical applications are central office, environmentally controlled vaults, environmentally controlled remote shelters, and environmentally controlled customer premise area.
GF	Ground, Fixed, Uncontrolled: Some environmental stress with limited maintenance. Typical applications are manholes, poles, remote terminals, and customer premise areas subject to shock, vibration, temperature, or atmospheric variations.

- **Software & Database**

  Analysis Software & Analysis Method

  Software Name : Relex Reliability Studio 2008

  Software Version : Relex Studio 2008

  Analysis Method

  The prediction method used was Telcordia SR-332, Issue 2,

  Parts Count

  Failure rate ($\boldsymbol{\lambda}$) = 10^9 hours (FITs)

  MTBF=1/$\boldsymbol{\lambda}$

  $\boldsymbol{\lambda}_{SSi} = \boldsymbol{\lambda}_{Gi}\ \mathbf{TT}_{Qi}\mathbf{TT}_{Si}\mathbf{TT}_{Ti}$

  Where $\boldsymbol{\lambda}_{Gi}$: Generic steady-state failure rate for device i

  $\mathbf{TT}_{Qi}$: Quality factor for device i

  $\mathbf{TT}_{Si}$: Stress factor for device i

  $\mathbf{TT}_{Ti}$: Temperature factor for device i

- **Calculation Parameter**

  Operation Temperature : 25℃

  Environment : Ground Benign, Controlled

  Operation Stress : 50% (Voltage, Current, Power)

  Method : Method I, Case 3

Products are advertised with MTBF up to 1 million hours in the market. Take one million hours as an example, the product's estimated life is 114 years. However, the current rapid progress of technology, advancement of flash storage device's manufacturing process research and development, and the supply period of former flash IC manufacturing processes are crucial to the actual life expectancy of flash products. In short, the MTBF of flash storage is for reference only. Good customer service and technical support provided by manufacturers is the most significant issue regarding to the life-span of products.

Remark:

All the details of testing and data are for reference only and do not imply any products performance as a result. MTBF is only an estimated date and is depends on both hardware and software. User shall not assume that all the products have the same MTBF as APRO estimates.

2. Product Specifications

For all the following specifications, values are defined at ambient temperature and nominal supply voltage unless otherwise stated.

2.1. System Environmental Specifications

Table 1: Environmental Specification

APRO SLC Industrial Micro IDE Flash (MIF) Module HERMIT-A Series		Standard Grade	Industrial Grade
		SP(B)MIFxxxG-HACTC	WP(B)MIFxxxG-HAITI
Temperature	Operating:	0ºC ~ +70ºC	-40ºC ~ +85ºC
	Non-operating:	-20ºC ~ +80ºC	-50ºC ~ +95ºC
Humidity	Operating & Non-operating:	10% ~ 95% non-condensing	
Vibration	Operating & Non-operating:	70 Hz to 2K Hz, 20G, 3 axes	
Shock	Operating & Non-operating:	0.5ms, 1500 G, 3 axes	

2.2. System Power Requirements

Table 2: Power Requirement

APRO SLC Industrial Micro IDE Flash (MIF) Module HERMIT-A Series	
DC Input Voltage (VCC) +5V ± 10% or +3.3V ± 10%	Operating @ +5V ± 10%
Reading Mode :	178.0 mA (max.)
Writing Mode :	142.5 mA (max.)
Idle Mode :	0.9 mA (max.)

2.3. System Performance

Table 3: System Performances

Data Transfer Mode supporting			- PIO mode: 0,1,2,3,4,5,6 (Default PIO-6) - MWDMA mode: 0,1,2 - UDMA Mode: 0,1,2,3,4 (Default UDMA-4)								
Data Transfer Rate To/Form Host			16.6Mybtes/sec burst under PIO Mode 4 66.6Mbytes/sec burst under UDMA-4 Mode								
Average Access Time			0.2 ms.(estimated)								
Maximum Performance	**Capacity**		**16MB**	**32MB**	**64MB**	**128MB**	**256MB**	**512MB**	**1GB**	**2GB**	**4GB**	**8GB**
	Sequential Read (MB/s)	**PIO-4**	4.6	4.6	4.6	4.6	4.6	4.6	4.7	4.7	4.7	4.6
		UDMA-4	17.15	17.15	17.41	18.3	18.2	20.3	39.5	38.1	37.8	37.8
	Sequential Write(MB/s)	**PIO-4**	4.2	4.2	4.2	4.2	4.2	4.0	4.6	4.6	4.6	4.0
		UDMA-4	5.94	5.94	6.02	11.4	16. 0	13.9	28.0	26.8	27.8	27.8

Note: The performance was measured using CrystalDiskMark by file size 500MB (QD32).

2.4. System Reliability

Table 4: System Reliability

Wear-leveling Algorithms	Static wear-leveling algorithms
Bad Blocks Management	Supported
ECC Technology	4-Bit per 512 bytes in an ECC block
Erase counts	NAND SLC Flash Cell Level : 60K P/E Cycles
Capacity	**TBW(TB)**
16MB	0.8
32MB	1.7
64MB	3.3
128MB	6.58
256MB	13.18
512MB	26.36
1GB	52.73
2GB	105.46
4GB	210.9
8GB	421.8

Note:

- *Samples were built using Toshiba SLC NAND flash.*
- *Test by sequential write.*
- *The endurance of SSD could be estimated based on user behavior, NAND endurance cycles, and write amplification factor. It is not guaranteed by flash vendor.*

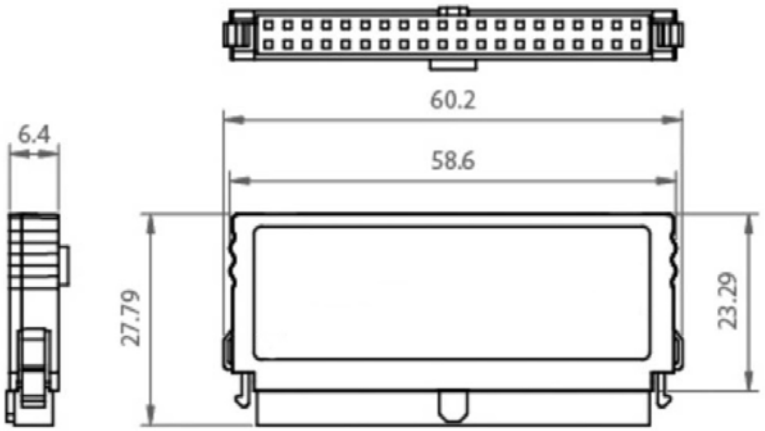
2.5. *Physical Specifications*

Refer to Table 5 and see Figure 3 for APRO SLC Industrial Micro IDE Flash (MIF) Module HERMIT-A Series physical specifications and dimensions.

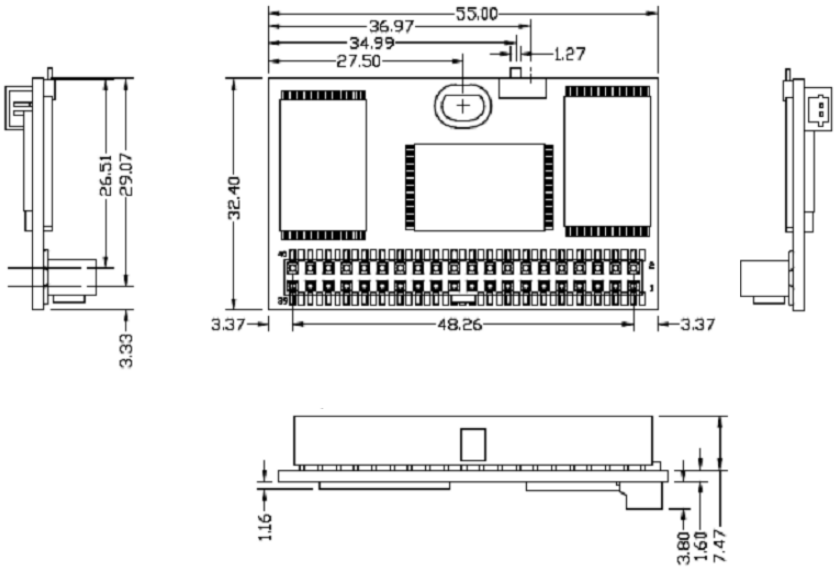
Table 5: Physical Specifications of APRO SLC Industrial Micro IDE Flash (MIF) Module HERMIT-A Series

40-pin MIF		
Orientation :	**Vertical Type**	**Horizontal Type**
Length:	60.20 mm	55.00 mm
Width:	27.79 mm	32.40 mm
Thickness:	6.40 mm	-
Weight:	20g / 0.70 oz.	15g / 0.52 oz.
44-pin MIF		
Orientation :	**Vertical Type**	**Horizontal Type**
Length:	50.25 mm	48.00 mm
Width:	27.27 mm	32.40 mm
Thickness:	5.80 mm	-
Weight:	15g / 0.52 oz.	12g / 0.42 oz.

40-pin Vertical Type MIF



40-pin Horizontal-leftward Type MIF



40-pin Horizontal-rightward Type MIF

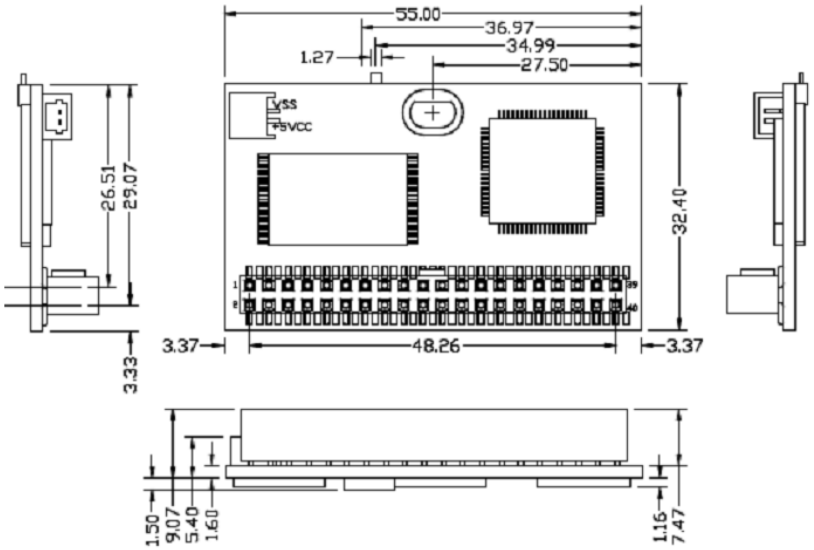
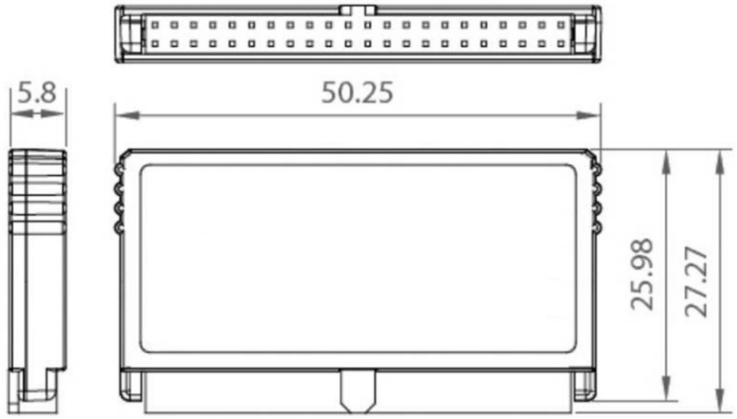
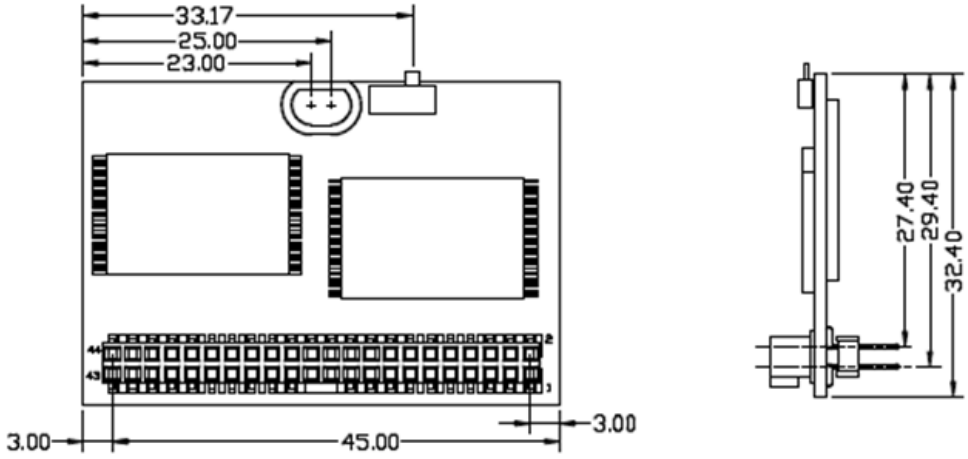


Figure 2: APRO SLC Industrial Micro IDE Flash (MIF) Module HERMIT-A Series 40-pin 3 form factors dimension.

44-pin Vertical Type MIF



44-pin Horizontal-leftward Type MIF



44-pin Horizontal-rightward Type MIF

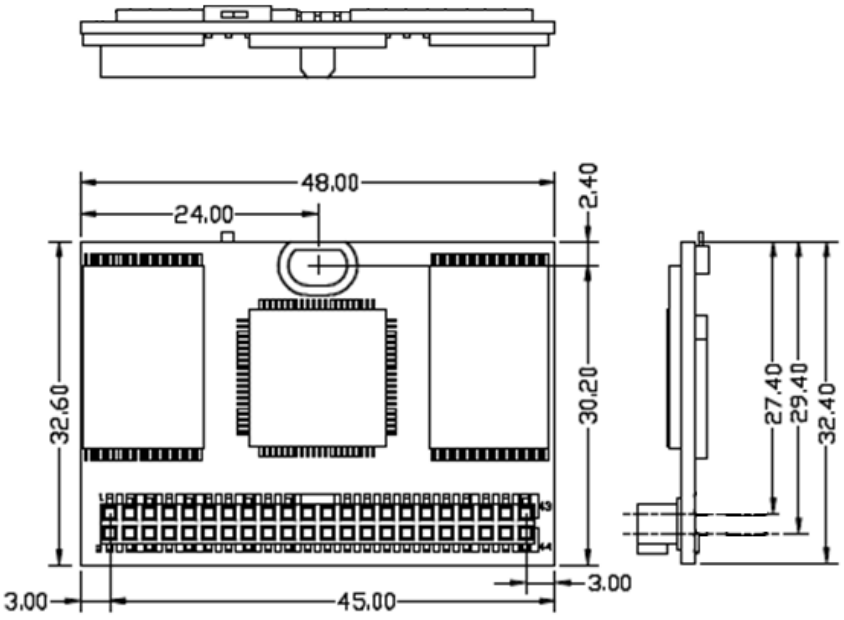


Figure 3: APRO SLC Industrial Micro IDE Flash (MIF) Module HERMIT-A Series 44-pin 3 form factors dimension.

2.6. *Conformal coating*

Conformal coating is a protective, dielectric coating designed to conform to the surface of an assembled printed circuit board. Commonly used conformal coatings include silicone, acrylic, urethane and epoxy. APRO applies only silicone on APRO storages products upon requested especially by customers. The type of silicone coating features good thermal shock resistance due to flexibility. It is also easy to apply and repair.

Conformal coating offers protection of circuitry from moisture, fungus, dust and corrosion caused by extreme environments. It also prevents damage from those Flash storages handling during construction, installation and use, and reduces mechanical stress on components and protects from thermal shock. The greatest advantage of conformal coating is to allow greater component density due to increased dielectric strength between conductors.

APRO use MIL-I-46058C silicon conformal coating

2.7. *Device Parameter*

The table 6 shows the specific capacity for the various models and the default number of heads, sectors/track and cylinders.

Table 6: Device Parameter of APRO SLC Industrial Micro IDE Flash (MIF) Module HERMIT-A Series

Unformatted Capacity	Cylinder	Head	Sector	LBA Total Sectors
16MB	248	4	32	31,744
32MB	500	8	16	64,000
64MB	500	8	32	112,000
128MB	480	16	32	245,760
256MB	984	16	32	503,808
512MB	1,001	16	63	1,009,008
1GB	2,002	16	63	2,018,016
2GB	4,003	16	63	4,035,024
4GB	8,006	16	63	8,070,048
8GB	16,000	16	63	16,128,000

3. Interface Description

3.1. APRO Micro IDE Flash interface (MIF)

APRO SLC Industrial Micro IDE Flash (MIF) Module HERMIT-A Series equipped Standard 40/44-pin connectors.

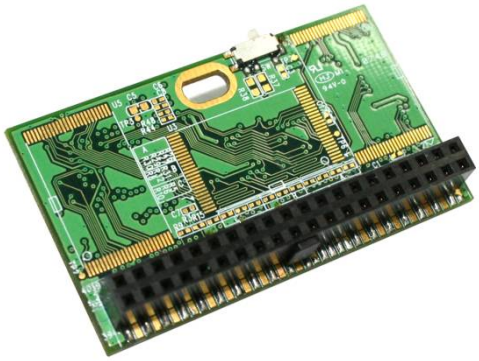
Vertical Type 40-pin IDE Connector	Horizontal Type 40-pin IDE Connector
	

Figure 4: Vertical & Horizontal Type 40-pin IDE Connector

Vertical Type 44-pin IDE Connector	Horizontal Type 44-pin IDE Connector
	

Figure 5: Vertical & Horizontal Type 44-pin IDE Connecto

3.2. Pin Assignments

Signals whose source is the host is designated as inputs while signals that the Industrial 40/44-pin micro IDE Flash (MIF) Module sources are outputs. The pin assignments are listed in below table 7.

Table 7: Pin Assignments

Pin No.	Signal Name	Description	Pin No.	Pin Name		Description
1	HRESET	Host Reset	**2**	GND		Ground
3	HDB[7]	Host Data Bit 7	**4**	HDB[8]		Host Data Bit 8
5	HDB[6]	Host Data Bit 6	**6**	HDB[9]		Host Data Bit 9
7	HDB[5]	Host Data Bit 5	**8**	HDB[10]		Host Data Bit 10
9	HDB[4]	Host Data Bit 4	**10**	HDB[11]		Host Data Bit 11
11	HDB[3]	Host Data Bit 3	**12**	HDB[12]		Host Data Bit 12
13	HDB[2]	Host Data Bit 2	**14**	HDB[13]		Host Data Bit 13
15	HDB[1]	Host Data Bit 1	**16**	HDB[14]		Host Data Bit 14
17	HDB[0]	Host Data Bit 0	**18**	HDB[15]		Host Data Bit 15
19	GND	Ground	**20**	40-pin MIF	VCC *1	Supply Voltage
				44-pin MIF	KEY[1]	Key-pin
21	DMARQ	DMA Request	**22**	GND		Ground
23	HIOW[3]	Host I/O Write	**24**	24		GND
	STOP[4]	Stop Ultra DMA burst				
25	HIOR[3]	Host I/O Read	**26**	GND		Ground
	HDMARDY[4]	Ultra DMA ready				
	HSTROBE[4]	Ultra DMA data strobe				
27	IORDY[3]	I/O Ready	**28**	CSEL		Cable select
	DDMARDY[4]	Ultra DMA ready				
	DSTROBE[4]	Ultra DMA data strobe				
29	DMACK	DMA Acknowledge	**30**	GND		Ground
31	INTRQ	Interrupt Request	**32**	IOCS16		CS I/O 16-Bit
33	HAB[1]	Host Address Bit 1	**34**	PDIAG		Passed Diagnostic
35	HAB[0]	Host Address Bit 0	**36**	HAB[2]		Host Address Bit 2
37	CS0	Chip Select 0	**38**	CS1		Chip Select 1
39	DASP	Drive Active	**40**	GND		Ground
41	VCC	Supply Voltage	**42**	VCC		Supply Voltage
43	GND	Ground	**44** *2	NC		Not Connected

***1**. According to ATA standard, the pin-20 in 40-pin module is defined as VCC to reduce the need for external power connector. Pin-20 in 44-pin module is defined as KEY.*

***2.** The 40-pin module does not include pins 41-44.*

NC = These pins are not connected within.

- *Signal usage in PIO & Multiword DMA mode.*
- *Signal usage in Ultra DMA mode.*

4. Installation Guide.

4.1. MIF Insertion and Removing

4.1.1. MIF Insertion

The connector of V-type MIF is very tight when plugging in, and it insures the MIF connection to motherboard properly. However, you have to be very careful to insert the MIF, especially V-type MIF, in right behavior. Blows are the important points for your attention to insert the MIF.

(1) Check the MIF housing to see if there are any damaged or loose parts and then check the female connector carefully if they are intact.

(2) Before inserting the MIF, please check each IDE pins on motherboard are perfect and straight.

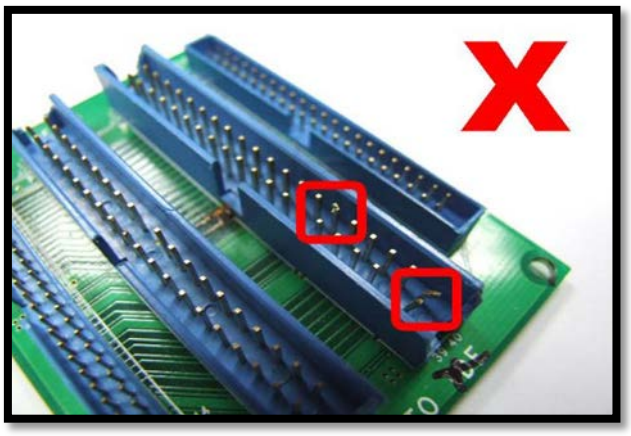


Figure 16: Defective IDE male Pins on Motherboard

Figure 17: Intact IDE male pins on Motherboard

(3) Any rude or wrong insertion will damage the both connectors of MIF and motherboard.

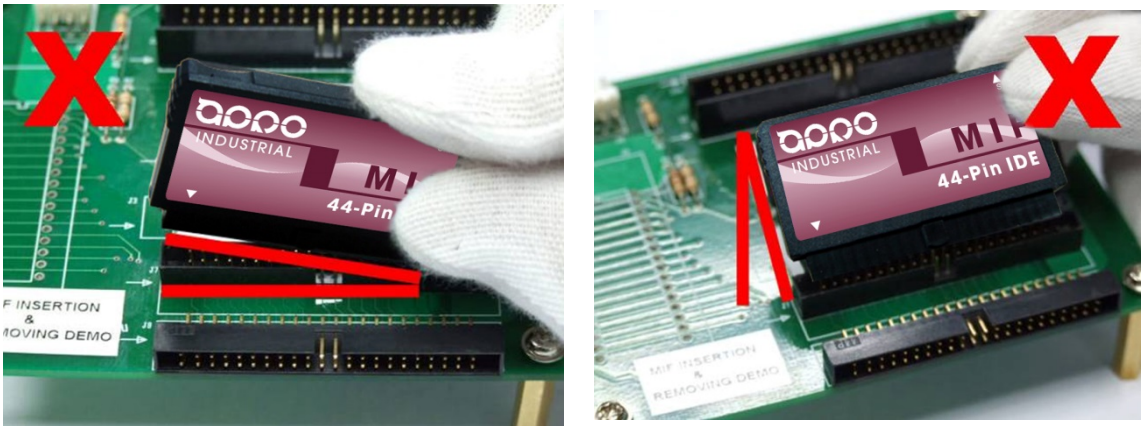


Figure 18: Wrong Insertions

(4) When plugging in, make sure pin-1 of MIF matches to pin 1 of IDE socket on motherboard. The two ends of connectors must be vertically aligned. Press it down gently and swing slightly a few times. If insertion is not smooth, DO NOT ATTEMPT TO INSERT FORCEFULLY.

4.1.2. MIF Removing

(1) Make sure the power is off before removing.

(2) As they are firmly attached, you can swing gently a few times to remove. DO NOT PULL IT OFF FORCE.

4.2. IDE Device Setup / Auto-Detection

Most BIOSs have an entry in the Standard Setup menu for each of the four IDE/ATA devices supported in a system (primary master, primary slave, secondary master, and secondary slave). For each one, you can enter a value for each setting in this section (type, size, cylinders, etc.).

Virtually all BIOSs now come with IDE device Auto-Detection. This comes in two forms:

- **Dynamic IDE Auto-Detection:** This is the fully automatic mode. You set one or more of the IDE devices (primary master, primary slave, etc.) on "Auto" and the BIOS will automatically re-detect and set the correct options for the drive each time you boot the PC. The BIOS will usually display on the screen what device it finds each time it auto-detects. For most people, this is the best way to go; it ensures that your BIOS always has the correct information about your hardware, and it removes any possibility of you installing a new drive but forgetting to set up the CMOS properly, or of changing a parameter by mistake in the setup program. Not all BIOSs offer this setting but most new ones do.

- **Manual IDE Auto-Detection:** This type of Auto-Detection is run from the BIOS setup program. You select Auto-Detection, and the BIOS will scan the IDE channels, and set the IDE parameters based on the devices it finds. When you save the BIOS settings, they are recorded permanently. The disadvantage of this is that if you change devices, you must return to the BIOS to re-auto-detect the new devices (unlike the dynamic Auto-Detection scheme, which does a fresh Auto-Detection each time you boot the PC). Virtually every BIOS created in the last 8 to 10 years offers manual Auto-Detection.

When you use dynamic Auto-Detection, the BIOS will normally "lock" the individual device settings that are being automatically set by the BIOS at boot time. Most systems that provide manual Auto-Detection will *not* lock the individual settings; they auto-detect, set the settings, and then let you change them if you want to. In most cases of course, you will not want to change what the BIOS detects.

Most BIOSs that allow dynamic Auto-Detection also allow manual Auto-Detection; the choice is yours. Using some sort of Auto-Detection for IDE/ATA devices is *strongly* recommended. It is the best way to reduce the chances of Module errors due to incorrect BIOS settings. It also provides immediate feedback of problems; if you can't auto-detect a drive from the BIOS, you know you have a problem even before you try to boot up.

4.3. Partition & Format

Before you install your operating system, you must first create a primary partition on the MIF on the system, and then format a file system on that partition. The Fdisk tool is an MS-DOS-based tool that you can use to prepare (partition) the MIF. You can use the Fdisk tool to create, change, delete, or display current partitions on the MIF, and then each allocated space on the MIF (primary partition, extended partition, or logical drive) is assigned a drive letter. Disk 1 may contain one extended partition, and a second MIF may contain a primary or extended partition. An extended partition may contain one or more logical MS-DOS drives.
After you use the Fdisk tool to partition MIF, use the Format tool to format those partitions with a file system. The file system File Allocation Table (FAT) allows the MIF to accept, store, and retrieve data. Windows 95 OEM Service Release 2 (OSR2), Windows 98, Windows 98 Second Edition, Windows Millennium Edition (Me), and Windows 2000 support the FAT16 and FAT32 file systems. When you run the Fdisk tool on a MIF that is larger than 512 megabytes (MB), you are prompted to choose one of the following file systems:

- **FAT16:** This file system has a maximum of 2 gigabytes (GB) for each allocated space or drive letter. For example, if you use the FAT16 file system and have a 6-GB MIF, you can have three drive letters (C, D, and E), each with 2 GB of allocated space.

- **FAT32:** This file system supports drives that are up to 2 terabytes in size and stores files on smaller sections of the MIF than the FAT16 file system does. This results in more free space on the MIF. The MIF file system does not support drives that are smaller than 512 MB.

When you run the Fdisk and format commands, the Master Boot Record (MBR) and file allocation tables are created. The MBR and file allocation tables store the necessary disk geometry that allows MIF to accept, store, and retrieve data.

Appendix A: Limited Warranty

APRO warrants your SLC Industrial Micro IDE Flash (MIF) Module HERMIT-A Series against defects in material and workmanship for the life of the drive. The warranty is void in the case of misuse, accident, alteration, improper installation, misapplication or the result of unauthorized service or repair. The implied warranties of merchantability and fitness for a particular purpose, and all other warranties, expressed or implied, except as set forth in this warranty, shall not apply to the products delivered. In no event shall APRO be liable for any lost profits, lost savings or other incidental or consequential damages arising out of the use of, or inability to use, this product.

BEFORE RETURNING PRODUCT, A RETURN MATERIAL AUTHORIZATION (RMA) MUST BE OBTAINED FROM APRO.

Product shall be returned to APRO with shipping prepaid. If the product fails to conform based on customers' purchasing orders, APRO will reimburse customers for the transportation charges incurred.

WARRANTY PERIOD:

- **SLC (Standard grade) 3 years / Within 60K Erasing Counts**
- **SLC (Industrial grade) 5 years / Within 60K Erasing Counts**

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