SQFlash
Technical Manual

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Revision History

Rev.	Date	History
0.1	2008/12/3	1. 1st draft
0.2	2008/12/8	1. Fixed the remark description.
0.3	2008/12/9	1. Increase the ATA command of the security function.
0.4	2008/12/12	1. Modify title
0.5	2008/12/31	1. Modify part number
0.6	2009/2/27	1. Fixed the part number
0.7	2009/5/25	1. Increase the General Description information.
0.8	2009/7/29	1. Define form template

1. Overview

The **CompactFlash Card** of the **SQFlash** is one of the best choices in the memory card market. It not only has an excellent performance but can also come in larger capacities do to CF card form factor. The CompactFlash Card does not require any additional mechanical parts, but have the properties of fully anti vibration and extremely low power consumption.

CompactFlash Card is one of the most popular cards today based on its high performance, good reliability and wide compatibility.

2. Controller Features

- **Support Host Interfaces**
  - PCMCIA / IDE Interface
  - (Support to PIO Mode 6 / Multi Word DMA Mode2 / Ultra DMA Mode 5)
  - Fully compatible with CompactFlash specification version 3.0
  - Fully compatible with PC Card Standard Release 8.0
  - Fully compatible with the IDE standard interface
  - Host Transfer Rate for PC Card / CompactFlash : 25MB/s (PIO6)
  - Host Transfer Rate for IDE standard interface: 100MB/s (UDMA5)
- **Build-In NAND Flash Memory Interface**
  - Build-in hardware ECC circuit (Reed-Solomon & B.C.H).
  - Support SLC (single level cell) NAND Flash Memory.
  - Support 2K bytes data per page and 4K bytes data per page NAND Flash Memory.
  - Support MLC (multi level cell) NAND flash.
- **1T RISC uP8051 RAM Mode**
  - Internal RAM: 256 Bytes.
  - External RAM: 24KB (On Chip)
- **Support SRAM Buffer (Dual Buffer Mode)**
  - A Buffer (512 Words)
  - B Buffer (512 Words)
  - CIS Buffer (256 bytes)
- **100-Pin TQFP Package**
- **Operating Voltage: 2.7~5.5V**
- **Power Saving implemented**

3. System Features

- **Capacities**
  - SLC type：1GB，2GB，4GB，8GB，16GB
- **Error Detection / Correction**
  - Built-in EDC/ECC up to 12 random bits error per 512 bytes.
- **Temperature Ranges**
  - Commercial Temperature
    - 0℃ to 70℃ for operating
    - -25℃ to 85℃ for storage
  - Industrial Temperature
    - -40℃ to 85℃ for operating
    - -40℃ to 85℃ for storage
- **Very low power consumption**
- **Low weight**
- **Noiseless**
- **Automatic error detection and retry capabilities**
- **Supports power down commands and sleep modes**
- **Compatible with all PC card services and socket services**
- **Host Transfer Rate for IDE standard interface : 100MB/s (UDMA5)**
- **Host Transfer Rate for PC Card / CompactFlash : 25MB/s (PIO6)**
- **Host interface : 8/16 bit access**
- **Auto sensing CF / ATA host interface**
- **3.3V / 5V operation voltage**
- **Mechanical Specification**
  - Shock：1,500G, Peak / 0.5ms
  - Vibration：20G, Peak / 10~2000Hz
- **Humidty**
  - Operating Humidity：5% ~ 95%
  - Non-Operating Humidity：5% ~ 95%
- **Endurance**
  - SLC type：> 5,000,000 program/erase cycles
- **MTBF**
  - > 6,000,000 hours
- **Insertions**
  - 10,000 times
- **NAND flash Data Retention**
  - 10 years

4. General Description

Advanced NAND Flash Controller

Advantech SQFlash CF card includes Bad Block Management Algorithm, Wear Leveling Algorithm and Error Detection / Correction Code (EDC/ECC) Algorithm.

Bad Block Management

Bad blocks are blocks that contain one or more invalid bits of which the reliability is not guaranteed. Bad blocks may be representing when flash is shipped and may developed during life time of the device.

Advantech SQFlash CF card implement a efficient bad block management algorithm to detect the factory produced bad blocks and manages any bad blocks that may develop over the life time of the device. This process is completely transparent to the user, user will not aware of the existence of the bad blocks during operation.

Wear Leveling

NAND Type flash have individually erasable blocks, each of which can be put through a finite number of erase cycles before becoming unreliable. It means after certain cycles for any given block, errors can be occurred in a much higher rate compared with typical situation. Unfortunately, in the most of cases, the flash media will not been used evenly. For certain area, like file system, the data gets updated much frequently than other area. Flash media will rapidly wear out in place without any rotation.

Wear leveling attempts to work around these limitations by arranging data so that erasures and re-writes are distributed evenly across the full medium. In this way, no single sector prematurely fails due to a high concentration of program/erase cycles.

Advantech SQFlash CF card provides advanced wear leveling algorithm, which can efficiently spread out the flash usage through the whole flash media area. By implement both dynamic and static wear leveling algorithms, the life expectancy of the flash media can be improved significantly.

Error Detection / Correction

Advantech SQFlash CF card utilizes BCH ECC Algorithm which offers one of the most powerful ECC algorithms in the industry. Built-in EDC/ECC up to 12 random bits error per 512 bytes.

Sophisticate Product Management Systems

Since industrial application require much more reliable devices compare with consumer product, a more sophisticated product management system become necessary for industrial customer requirement. The key to providing reliable devices is product traceability and failure analysis system. By implement such systems end customer can expect much more reliable product.

5. Pin Assignment and Description

5.1 Compact Flash Interface Pin Assignments

PC Card Memory Mode			PC Card I/O Mode			True IDE Mode		
Pin #	Signal Name	Pin Type	Pin #	Signal Name	Pin Type	Pin #	Signal Name	Pin Type
1	GND		1	GND		1	GND	I/O
2	D03	I/O	2	D03	I/O	2	D03	I/O
3	D04	I/O	3	D04	I/O	3	D04	I/O
4	D05	I/O	4	D05	I/O	4	D05	I/O
5	D06	I/O	5	D06	I/O	5	D06	I/O
6	D07	I/O	6	D07	I/O	6	D07	I
7	-CE1	I	7	-CE1	I	7	-CSO	I
8	A10	I	8	A10	I	8	A10	I
9	-OE	I	9	-OE	I	9	-ATA SEL	I
10	A09	I	10	A09	I	10	A09	I
11	A08	I	11	A08	I	11	A08	I
12	A07	I	12	A07	I	12	A07	
13	VCC		13	VCC		13	VCC	I
14	A06	I	14	A06	I	14	A06	I
15	A05	I	15	A05	I	15	A05	I
16	A04	I	16	A04	I	16	A04	I
17	A03	I	17	A03	I	17	A03	I
18	A02	I	18	A02	I	18	A02	I
19	A01	I	19	A01	I	19	A01	I
20	A00	I	20	A00	I	20	A00	I/O
21	D00	I/O	21	D00	I/O	21	D00	I/O
22	D01	I/O	22	D01	I/O	22	D01	I/O
23	D02	I/O	23	D02	I/O	23	D02	O
24	WP	O	24	-IOIS16	O	24	-IOIS16	O
25	-CD2	O	25	-CD2	O	25	-CD2	O
26	-CD1	O	26	-CD1	O	26	-CD1	I/O
27	D11	I/O	27	D11	I/O	27	D11	I/O
28	D12	I/O	28	D12	I/O	28	D12	I/O
29	D13	I/O	29	D13	I/O	29	D13	I/O
30	D14	I/O	30	D14	I/O	30	D14	I/O

PC Card Memory Mode			PC Card I/O Mode			True IDE Mode		
Pin #	Signal Name	Pin Type	Pin #	Signal Name	Pin Type	Pin #	Signal Name	Pin Type
31	D15	I/O	31	D15	I/O	31	D15	I
32	-CE2	I	32	-CE2	I	32	-CS1	O
33	-VS1	O	33	-VS1	O	33	-VS1	I
34	-IORD	I	34	-IORD	I	34	-IORD	I
35	-IOWR	I	35	-IOWR	I	35	-IOWR	I
36	-WE	I	36	-WE	I	36	-WE	I
37	RDY/BSY	O	37	IREQ	O	37	INTRQ	
38	VCC		38	VCC		38	VCC	I
39	-CSEL	I	39	-CSEL	I	39	-CSEL	I
40	-VS2	O	40	-VS2	O	40	-VS2	I
41	RESET	I	41	RESET	I	41	RESET	O
42	-WAIT	O	42	-WAIT	O	42	IORDY	O
43	-INPACK	O	43	-INPACK	O	43	-INPACK	I
44	-REG	I	44	-REG	I	44	-REG	I/O
45	BVD2	I/O	45	-SPKR	I/O	45	-DASP	I/O
46	BVD1	I/O	46	-STSCHG	I/O	46	-PDIAG	I/O
47	D08	I/O	47	D08	I/O	47	D08	I/O
48	D09	I/O	48	D09	I/O	48	D09	I/O
49	D10	I/O	49	D10	I/O	49	D10	
50	GND		50	GND		50	GND	

Remark :

1. WE should be connected to VCC in True IDE mode.
2. CSEL is input pin for master/slave selection used in True IDE mode.

5.2 Signal Descriptions

Signal Name	Dir.	Pin	Description
BVD2 (PC Card Memory Mode)	I/O	45	This output line is always driven to a high state in Memory Mode since a battery is not required for this product
-SPKR (PC CARD I/O Mode)			This output line is always driven to a high state in I/O Mode since this product does not support the audio function
-DASP (True IDE Mode)			In the True IDE Mode, this input/output is the Disk Active/Slave Present signal in the Master/Slave handshake protocol
-CD1,-CD2 (PC Card Memory Mode)	O	26, 25	These card detect pins are connected to the ground on the CompactFlash™ Storage Card. They are used by the host to determine that the CompactFlash™ Storage Card is fully inserted into its socket.
-CD1,-CD2 (PC Card I/O Mode)			The signal is the same for all modes
-CD1,-CD2 (True IDE Mode)			The signal is the same for all modes
D[15:0] (PC Card Memory Mode)	I/O	31, 30, 29, 28, 27, 49, 48, 47, 6, 5, 4, 3, 2, 23, 22, 21	These lines carry the Data, Commands, and Status information between the host and the controller. D00 is the LSB of the Odd Byte of the World
D[15:0] (PC Card I/O Mode)			The signal is the same as the PC Card Memory Mode signal.
D[15:0] (True IDE Mode)			In True IDE Mode, all Task File operations occur in byte mode on the lower order bus D00-D07 while all data transfers are 16 bit using D00-D15.
-IOWR (PC Card Memory Mode)	I	35	This signal is not used in this mode.
-IOWR (PC Card I/O Mode)			The I/O Write strobe pulse is used to clock I/O data on the Card Data bus into the CompactFlash™ Storage Card or CF+ Card controller registers when the CompactFlash™ Storage Card or CF+ Card is configured to use the I/O interface. The clocking shall occur on the negative to positive edge of the signal (trailing edge).
-IOWR (True IDE Mode – Except Ultra DMA Protocol Active)			In True IDE Mode, while Ultra DMA mode protocol is not active, this signal has the same function as in PC Card I/O Mode. When Ultra DMA mode protocol is supported, this signal must be negated before entering Ultra DMA mode protocol.
STOP (True IDE Mode – Ultra DMA Protocol Active)			In True IDE Mode, while Ultra DMA mode protocol is active, the assertion of this signal causes the termination of the Ultra DMA burst.

Signal Name	Dir.	Pin	Description
-IORD (PC Card Memory Mode)	I	34	This signal is not used in this mode.
-IORD (PC Card I/O Mode)			This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the CompactFlash™ Storage Card or CF+ Card when the card is configured to use the I/O interface.
-IORD (True IDE Mode – Except Ultra DMA Protocol Active)			In True IDE Mode, while Ultra DMA mode is not active, this signal has the same function as in PC Card I/O Mode.
-HDMARDY (True IDE Mode – In Ultra DMA Protocol DMA Read)			In True IDE Mode when Ultra DMA mode DMA Read is active, this signal is asserted by the host to indicate that the host is ready to receive Ultra DMA data-in burst. The host may negate –HDMARDY to pause an Ultra DMA transfer.
-HSTROBE (True IDE Mode – In Ultra DMA Protocol DMA Write)			In True IDE Mode when Ultra DMA mode DMA Write is active, this signal is the data out strobe generated by the host. Both the rising and falling edge of HSTROBE cause data to be latched by the device. The host may stop generating HSTROBE edges to pause an Ultra DMA data-out burst.
-WE (PC Card Memory Mode)	I	36	This signal driven by the host and used for strobing memory write data to the registers of the CompactFlash™ Storage Card when the card is configured in the memory interface mode. It is also used for writing the configuration registers.
-WE (PC Card I/O Mode)			In PC Card I/O Mode, this signal is used for writing the configuration registers.
-WE (True IDE Mode)			In True IDE Mode this input signal is not used and should be connected to VCC by the host.
-OE (PC Card Memory Mode)	I	9	This is an Output Enable strobe generated by the host interface. It is used to read data from the CompactFlash™ Storage Card in Memory Mode and to read the CIS and configuration registers.
-OE (PC Card I/O Mode)			In PC Card I/O Mode this input, this signal is used to read the CIS and configuration registers.
-OE (True IDE Mode)			To enable True IDE Mode this input should be grounded by the host.

Signal Name	Dir.	Pin	Description
RDY/-BSY (PC Card Memory Mode)	O	37	In Memory Mode this signal is set high when the CompactFlash™ Storage Card is ready to accept a new data transfer operation and held low when the card is busy. The Host memory card socket must provide a pull-up resistor. At power up and at Reset, the RDY/-BSY is held low (busy) until the CompactFlash™ Storage Card has completed its power up or reset function. No access of any type should be made to the CompactFlash™ Storage Card during this time. The RDY/-BSY signal is held high (disabled from being busy) whenever the following condition is true: The CompactFlash™ Storage Card has been powered up with +RESET continuously disconnected or asserted.
-IREQ (PC Card I/O Mode)			I/O Operation- After the CompactFlash™ Storage has been configured for I/O operation, this signal is used as –Interrupt Request. This line is strobed low to generate a pulse mode interrupt or held low for a level mode interrupt.
INTRQ (True IDE Mode)			In True IDE Mode signal is an active high Interrupt Request to the host.
A[10:0] (PC Card Memory Mode)	I	8, 10, 11, 12, 14, 15, 16, 17, 18, 19, 20	These address lines along with the –REG signal are used to select the following: The I/O port address registers within the CompactFlash™ Storage Card, the memory mapped port address registers within the CompactFlash™ Storage Card, a byte in the card's information structure and its configuration control and status registers.
A[10:0] (PC Card I/O Mode)			The signal is the same as the PC Card Memory Mode signal.
A[2:0] (True IDE Mode)			In True IDE Mode only HA[2:0] are used to select the one of eight registers in the Task File, the remaining address lines should be grounded by the host .
-CE1,-CE2 (PC Card Memory Mode) Card Enable	I	7, 32	These input signals are used to select the card and to indicate to the card whether a byte or a word operation is being performed. –CE2 always accesses the odd byte of the word. –CE1 accesses the even byte or the Odd byte of the word depending on the A0 and –CE2. A multi-plexing scheme based on A0, -CE1, -CE2 allows 8 bit hosts to access all data on D0-D7.
-CE1,-CE2 (PC Card I/O Mode) Card Enable			This signal is the same as the PC Card Memory Mode signal.
-CS0,-CS1 (True IDE Mode)			In the True IDE Mode CS0 is the chip select for the task file registers while CS2 is used to select the Alternate Status Register and the Device Control Register.
-CSEL (PC Card Memory Mode)	I	39	This signal is not used for this mode.
-CSEL (PC Card I/O Mode)			This signal is not used for this mode.
-CSEL (True IDE Mode)			This internally pulled up signal is used to configure this device as a Master or a Slave when configured in the True IDE Mode. When this pin is grounded, this device is configured as a Master. When the pin is open, this device is configured as a Slave.

Signal Name	Dir.	Pin	Description
-REG (PC Card Memory Mode) Attribute Memory Select	I	44	This signal is used during Memory Cycles to distinguish between Common Memory and Register (Attribute) Memory accesses. High for Common Memory, Low for Attribute Memory
-REG (PC Card I/O Mode)			The signal shall also be active (low) during I/O Cycles when the I/O address is on the Bus.
-DMACK (True IDE Mode)			This is a DMA Acknowledge signal that is asserted by the host in response to DMARQ to initiate DMA transfers. While DMA operations are not active, the card shall ignore -DMACK signal, including a floating condition. If DMA operation is not supported by a True IDE Mode only host, this signal should be driven high or connected to VCC by the host. A host that does not support DMA mode and implements both PCMCIA and True-IDE modes of operation need not alter the PCMCIA mode connections while in True-IDE mode as long as this does not prevent proper operation all modes.
WP (PC Card Memory Mode) Write Protect	O	24	Memory Mode- The CompactFlash™ Storage Card does not have a write protect switch. This signal is held low after the addressed port.
-IOIS 16 (PC Card I/O Mode)			I/O Operation- When the CompactFlash™ Storage Card is configured for I/O Operation Pin 24 is used for the –I/O Selected is a 16 Bit Port (-IOIS16) function. A Low signal indicates that a 16 bit or odd byte only operation can be performed at the addressed port.
-IOIS 16 (True IDE Mode)			In True IDE Mode this output signal is asserted low when this device is expecting a word data transfer cycle.

Signal Name	Dir.	Pin	Description
-INPACK (PC Card Memory Mode)	O	43	This signal is not used in this mode.
-INPACK (PC Card I/O Mode) Input Acknowledge			The Input Acknowledge signal is asserted by the CompactFlash™ Storage Card or CF+ Card when the card is selected and responding to an I/O read cycle at the address that is on the address bus. This signal is used by the host to control the enable of any input data buffers between CompactFlash™ Storage Card or CF+ Card and the CPU.
-DMARQ (True IDE Mode)			This signal is a DMA Request that is used for DMA data transfers between host and device. It shall be asserted by the device when it is ready to transfer data to or from the host. For Multiword DMA transfers, the direction of data transfer is controlled by –IORD and –IOWR. This signal is used in a handshake manner with –DMACK, ie: the device shall wait until the host asserts –DMACK before negating DMARQ, and re-asserting DMARQ if there is more data to transfer. DMARQ shall not be driven when the device is not selected. While a DMA operation is in progress, -CS0 and –CS1 shall be held negated and the width of the transfers shall be 16 bits. If there is no hardware support for DMA mode in the host, this output signal is not used and should not be connected at the host. In this case, the BIOS must report that DMA mode is not supported by the host so that device drivers will not attempt DMA mode. A host that does not support DMA mode and implements both PCMCIA and True-IDE modes of operation need not alter the PCMCIA mode connections while in True-IDE mode as long as this does not prevent proper operation in any mode.
BVD1 (PC Card Memory Mode)	I/O	46	This signal is asserted high as the BVD1 signal since a battery is not used with this product.
-STSCHG (PC Card I/O Mode) Status Changed			This signal is asserted low to alert the host to changes in the RDY/-BSY and Write Protect states, while the I/O interface is configured. Its use is controlled by the Card Config and Status Register.
-PDIAG (True IDE Mode)			In the True IDE Mode, this input / output is the Pass Diagnostic signal in the Master / Slave handshake protocol.

Signal Name	Dir.	Pin	Description
-WAIT (PC Card Memory Mode)	O	42	The –WAIT signal is driven low by the CompactFlash™ Storage Card or CF+ Card to signal the host to delay completion of a memory or I/O cycle that is in progress.
-WAIT (PC Card I/O Mode)			This signal is the same as the PC Card Memory Mode signal.
IORDY (True IDE Mode – Except Ultra DMA Mode)			In True IDE Mode, except in Ultra DMA modes, this output signal may be used as IORDY.
-DDMARDY (True IDE Mode – Ultra DMA Write Mode)			In True IDE Mode, when Ultra DMA mode DMA Write is active, this signal is asserted by the host to indicate that the device is ready to receive Ultra DMA data-in bursts. The device may negate –DDMARDY to pause an Ultra DMA transfer.
-DSTROBE (True IDE Mode – Ultra DMA Read Mode)			In True IDE Mode, when Ultra DMA mode DMA Write is active, this signal is the data out strobe generated by the device. Both the rising and falling edge of DSTROBE cause data to be latched by the host. The device may stop generating DSTROBE edges to pause an Ultra DMA data-out burst.
GND (PC Card Memory Mode)	--	1, 50	Ground.
GND (PC Card I/O Mode)			This signal is the same for all modes.
GND (True IDE Mode)			This signal is the same for all modes.
VCC (PC Card Memory Mode)	--	13, 38	+5V, +3.3V power
VCC (PC Card I/O Mode)			This signal is the same for all modes.
VCC (True IDE Mode)			This signal is the same for all modes.
RESET (PC Card Memory Mode)	I	41	When the pin is high this signal Resets the CompactFlash™ Storage Card. The CompactFlash™ Storage Card is Reset only at power up if this pin is left high or open from power up. The CompactFlash™ Storage Card is also Reset when the Soft Reset bit in the Card Configuration Option Register is set.
RESET (PC Card I/O Mode)			The signal is the same as the PC Card Memory Mode signal.
RESET (True IDE Mode)			In the True IDE Mode this input pin is the active low hardware reset from the host.
-VS1 **-VS2** (PC Card Memory Mode)	O	33 40	Voltage Sense Signals. –VS1 is grounded so that the CompactFlash™ Storage Card CIS can be read at 3.3 volts and –VS2 is reserved by PCMCIA for a secondary voltage.
-VS1 **-VS2** (PC Card I/O Mode)			This signal is the same for all modes.
-VS1 **-VS2** (True IDE Mode)			This signal is the same for all modes.

6. Identify Drive Information

Word Address	Default Value	Total Bytes	Data Field Type Information
0	044AH	2	General configuration bit-significant information
1	XXXX	2	Default number of cylinders
2	0000H	2	Reserved
3	XXXX	2	Default number of heads
4	0000H	2	Retired
5	0200H	2	Retired
6	XXXX	2	Default number of sectors per track
7-8	XXXXh	4	Number of sectors per card
9	0000H	2	Retired
10-19	XXXX	20	Serial Number in ASCII
20	0002H	2	Retired
21	0002H	2	Retired
22	0004H	2	Obsolete
23-26	XXXX	8	Firmware revision in ASCII
27-46	XXXX	40	Model number in ASCII
47	0001H	2	Maximum number of sector that shall be transferred on Read/Write Multiple commands
48	0000H	2	Reserved
49	0300H	2	Obsolete
50	0000H	2	Reserved
51	0200H	2	PIO data transfer cycle timing mode 2
52	0000H	2	Retired
53	0007H	2	Word 54-58, 64-70 and 88 are valid
54	XXXX	2	Current numbers of cylinders
55	XXXX	2	Current numbers of heads
56	XXXX	2	Current sectors per track
57-58	XXXX	4	Current capacity in sectors (LBAs)(Word 57= LSW, Word 58= MSW)
59	0101H	2	Multiple sector setting is valid
60-61	XXXX	4	Total number of sectors addressable in LBA Mode
62	0000H	2	Retired
63	0007H	2	Multiword DMA mode 2 and below are supported
64	0003H	2	Advance PIO transfer modes supported
65	0078H	2	Minimum Multiword DMA transfer cycle time 120nsec
66	0078H	2	Manufacturer's recommended Multiword DMA transfer cycle time 120nsec
67	0078H	2	Minimum PIO transfer cycle time without flow control 120nsec
68	0078H	2	Minimum PIO transfer cycle time with IORDY flow control 120nsec
69-81	0000H	26	Reserved
82	0002H	2	Supports Security Mode feature set
83-87	0000H	10	Reserved
88	0X3FH	2	Ultra DMA mode 5 and below are supported
89-127	0000H	78	Reserved
128	0021H	2	Enhanced security erase supported
129-159	0000H	62	Reserved vendor unique bytes
160-255	0000H	192	Reserved

7. CIS information

Address	Data	Description of contents	CIS function
000H	01H	CISTPL_DEVICE	Tuple code
002H	04H	TPL_LINK	Tuple link
004H	DFH	Device information	Tuple data
006H	4AH	Device information	Tuple data
008H	01H	Device information	Tuple data
00AH	FFH	END MARKER	End of Tuple
00CH	1CH	CISTPL_DEVICE_OC	Tuple code
00EH	04H	TPL_LINK	Tuple link
010H	02H	Conditions information	Tuple data
012H	D9H	Device information	Tuple data
014H	01H	Device information	Tuple data
016H	FFH	END MARKER	End of Tuple
018H	18H	CISTPL_JEDEC_C	Tuple code
01AH	02H	TPL_LINK	Tuple link
01CH	DFH	PCMCIA's manufacturer's JEDEC ID code	Tuple data
01EH	01H	PCMCIA's JEDEC device code	Tuple data
020H	20H	CISTPL_MANFID	Tuple code
022H	04H	TPL_LINK	Tuple link
024H	0AH	Low byte of manufacturer's ID code	Tuple data
026H	00H	High byte of manufacturer's ID code	Tuple data
028H	00H	Low byte of product code	Tuple data
02AH	00H	High byte of product code	Tuple data
02CH	15H	CISTPL_VERS_1	Tuple code
02EH	13H	TPL_LINK	Tuple link
030H	04H	TPLLV1_MAJOR	Tuple data
032H	01H	TPLLV1_MINOR	Tuple data
034H	50H	'P ' (Vender Specific Strings)	Tuple data
036H	48H	' H ' (Vender Specific Strings)	Tuple data
038H	49H	' I ' (Vender Specific Strings)	Tuple data
03AH	53H	'S ' (Vender Specific Strings)	Tuple data
03CH	4FH	' O ' (Vender Specific Strings)	Tuple data
03EH	4EH	'N ' (Vender Specific Strings)	Tuple data

Address	Data	Description of contents	CIS function
040H	00H	Null Terminator	Tuple data
042H	43H	'C ' (Vender Specific Strings)	Tuple data
044H	46H	' F ' (Vender Specific Strings)	Tuple data
046H	20H	' ' (Vender Specific Strings)	Tuple data
048H	43H	' C ' (Vender Specific Strings)	Tuple data
04AH	61H	' a ' (Vender Specific Strings)	Tuple data
04CH	72h	' r ' (Vender Specific Strings)	Tuple data
04EH	64H	' d ' (Vender Specific Strings)	Tuple data
050H	00H	Null Terminator	Tuple data
052H	00H	Reserved (Vender Specific Strings)	Tuple data
054H	FFH	END MARKER	End of Tuple
056H	21H	CISTPL_FUNCID	Tuple code
058H	02H	TPL_LINK	Tuple link
05AH	04H	IC Card function code	Tuple data
05CH	01H	System initialization bit mask	Tuple data
05EH	22H	CISTPL_FUNCE	Tuple code
060H	02H	TPL_LINK	Tuple link
062H	01H	Type of extended data	Tuple data
064H	01H	Function information	Tuple data
066H	22H	CISTPL_FUNCE	Tuple code
068H	03H	TPL_LINK	Tuple link
06AH	02H	Type of extended data	Tuple data
06CH	0CH	Function information	Tuple data
06EH	0FH	Function information	Tuple data
070H	1AH	CISTPL_CONFIG	Tuple code
072H	05H	TPL_LINK	Tuple link
074H	01H	Size field	Tuple data
076H	03H	Index number of last entry	Tuple data
078H	00H	Configuration register base address (Low)	Tuple data
07AH	02H	Configuration register base address (High)	Tuple data
07CH	0FH	Configuration register present mask	Tuple data
07EH	1BH	CISTPL_CFTABLE_ENTRY	Tuple code
080H	08H	TPL_LINK	Tuple link

Address	Data	Description of contents	CIS function
082H	C0H	Configuration Index Byte	Tuple data
084H	C0H	Interface Descriptor	Tuple data
086H	A1H	Feature Select	Tuple data
088H	01H	Vcc Selection Byte	Tuple data
08AH	55H	Nom V Parameter	Tuple data
08CH	08H	Memory length (256 byte pages)	Tuple data
08EH	00H	Memory length (256 byte pages)	Tuple data
090H	20H	Misc features	Tuple data
092H	1BH	CISTPL_CFTABLE_ENTRY	Tuple code
094H	06H	TPL_LINK	Tuple link
096H	00H	Configuration Index Byte	Tuple data
098H	01H	Feature Select	Tuple data
09AH	21H	Vcc Selection Byte	Tuple data
09CH	B5H	Nom V Parameter	Tuple data
09EH	1EH	Nom V Parameter	Tuple data
0A0H	4DH	Peak I Parameter	Tuple data
0A2H	1BH	CISTPL_CFTABLE_ENTRY	Tuple code
0A4H	0AH	TPL_LINK	Tuple link
0A6H	C1H	Configuration Index Byte	Tuple data
0A8H	41H	Interface Descriptor	Tuple data
0AAH	99H	Feature Select	Tuple data
0ACH	01H	Vcc Selection Byte	Tuple data
0AEH	55H	Nom V Parameter	Tuple data
0B0H	64H	I/O Parameter	Tuple data
0B2H	F0H	IRQ parameter	Tuple data
0B4H	FFH	IRQ request mask	Tuple data
0B6H	FFH	IRQ request mask	Tuple data
0B8H	20H	Misc features	Tuple data
0BAH	1BH	CISTPL_CFTABLE_ENTRY	Tuple code
0BCH	06H	TPL_LINK	Tuple link
0BEH	01H	Configuration Index Byte	Tuple data
0C0H	01H	Feature Select	Tuple data
0C2H	21H	Vcc Selection Byte	Tuple data

Address	Data	Description of contents	CIS function
0C4H	B5H	Nom V Parameter	Tuple data
0C6H	1EH	Nom V Parameter	Tuple data
0C8H	4DH	Peak I parameter	Tuple data
0CAH	1BH	CISTPL_CFTABLE_ENTRY	Tuple code
0CCH	0FH	TPL_LINK	Tuple link
0CEH	C2H	Configuration Index Byte	Tuple data
0D0H	41H	Interface Descriptor	Tuple data
0D2H	99H	Feature Select	Tuple data
0D4H	01H	Vcc Selection Byte	Tuple data
0D6H	55H	Nom V Parameter	Tuple data
0D8H	EAH	I/O parameter	Tuple data
0DAH	61H	I/O range length and size	Tuple data
0DCH	F0H	Base address	Tuple data
0DEH	01H	Base address	Tuple data
0E0H	07H	Address length	Tuple data
0E2H	F6H	Base address	Tuple data
0E4H	03H	Base address	Tuple data
0E6H	01H	Address length	Tuple data
0E8H	EEH	IRQ parameter	Tuple data
0EAH	20H	Misc features	Tuple data
0ECH	1BH	CISTPL_CFTABLE_ENTRY	Tuple code
0EEH	06H	TPL_LINK	Tuple link
0F0H	02H	Configuration Index Byte	Tuple data
0F2H	01H	Feature Select	Tuple data
0F4H	21H	Vcc Selection Byte	Tuple data
0F6H	B5H	Nom V Parameter	Tuple data
0F8H	1EH	Nom V Parameter	Tuple data
0FAH	4DH	Peak I Parameter	Tuple data
0FCH	1BH	CISTPL_CFTABLE_ENTRY	Tuple code
0FEH	0FH	TPL_LINK	Tuple link
100H	C3H	Configuration Index Byte	Tuple data
102H	41H	Interface Descriptor	Tuple data
104H	99H	Feature Select	Tuple data

Address	Data	Description of contents	CIS function
106H	01H	Vcc Selection Byte	Tuple data
108H	55H	Nom V Parameter	Tuple data
10AH	EAH	I/O parameter	Tuple data
10CH	61H	I/O range length and size	Tuple data
10EH	70H	Base address	Tuple data
110H	01H	Base address	Tuple data
112H	07H	Address length	Tuple data
114H	76H	Base address	Tuple code
116H	03H	Base address	Tuple link
118H	01H	Address length	Tuple data
11AH	EEH	IRQ parameter	Tuple data
11CH	20H	Misc features	Tuple data
11EH	1BH	CISTPL_CFTABLE_ENTRY	Tuple code
120H	06H	TPL_LINK	Tuple link
122H	03H	Configuration Index Byte	Tuple data
124H	01H	Feature Select	Tuple data
126H	21H	Vcc Selection Byte	Tuple data
128H	B5H	Nom V Parameter	Tuple data
12AH	1EH	Nom V Parameter	Tuple data
12CH	4DH	Peak I Parameter	Tuple data
12EH	14H	CISTPL_NO_LINK	Tuple code
130H	00H	TPL_LINK	Tuple link
132H	FFH	CISTPL_END	End of Tuple
134H	FFH	CISTPL_END	End of Tuple
136H	FFH	CISTPL_END	End of Tuple
138H	FFH	CISTPL_END	End of Tuple
13AH	FFH	CISTPL_END	End of Tuple

8. Power Management

CF Card provides automatic power saving mode. There are four modes on this system.

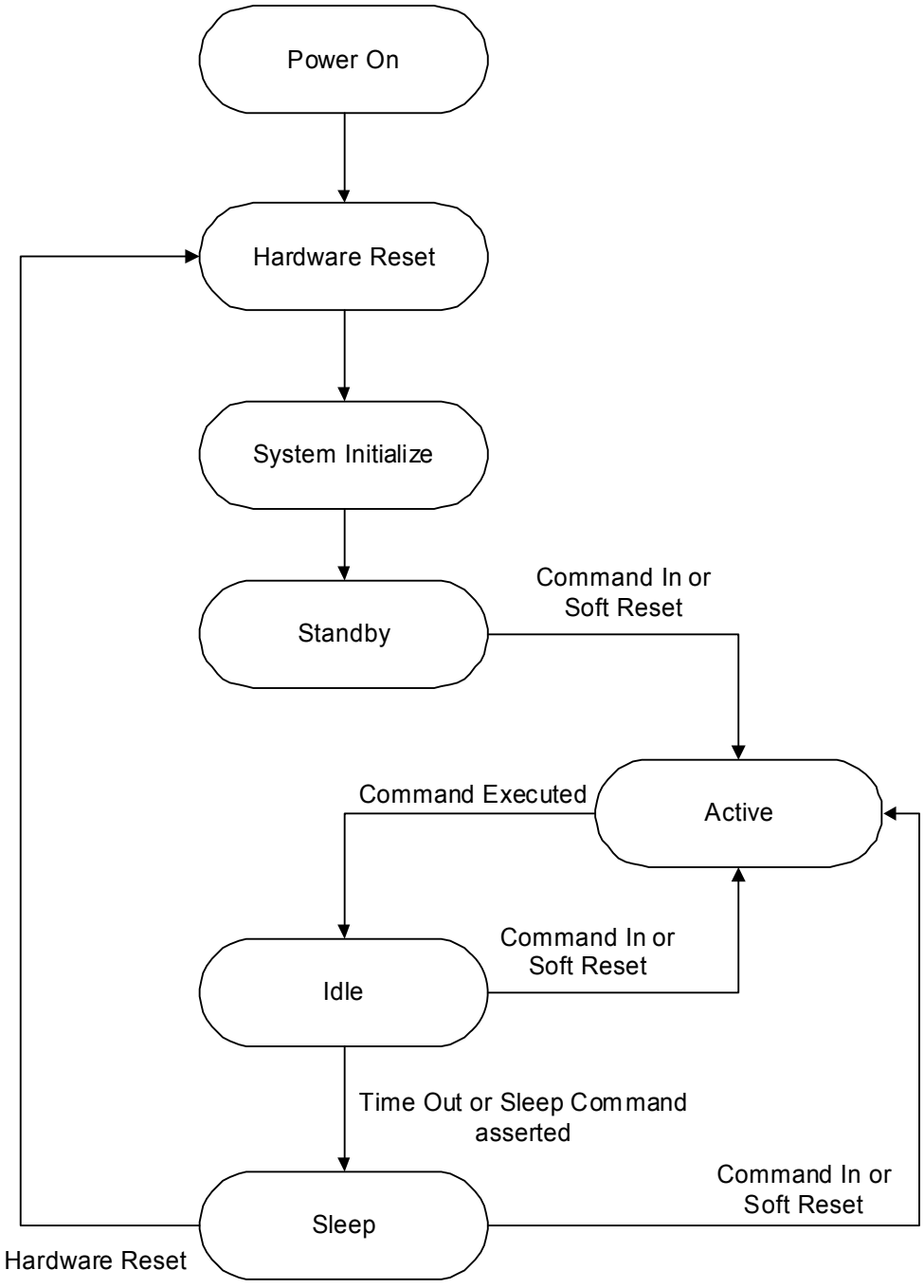
Standby Mode: When CF Card finishes the initialization routine after power reset, it goes into Standby Mode and wait for Command In or Soft Reset.

Active Mode: If CF Card received any Command In or Soft Reset, it goes into Active Mode. In Active Mode, it is capable to execute any ATA commands. The power consumption is the greatest in this mode.

Idle Mode: After CF Card executed any ATA Commands or Soft Reset, it goes into Idle Mode. Power consumption is reduced from Active Mode.

Sleep Mode: The CF Card will enter Sleep Mode if there is no Command In or Soft Reset from the host. Sleep Mode provides the lowest power consumption. During Sleep Mode, the system main clock is stopped. This mode can be waked up from hardware reset, software reset or any ATA command asserted.

8.1 Power Saving Flow



9. ATA Command Set

[Command Set List]

No.	Command set	Code	FR	SC	SN	CY	DR	HD	LBA
1	CHECK POWER MODE	98h,E5h	N	N	N	N	Y	N	N
2	EXECUTE DEVICE DIAGNOSTIC	90h	N	N	N	N	N	N	N
3	IDENTIFY DEVICE	Ech	N	N	N	N	Y	N	N
4	IDLE	97h,E3h	N	Y	N	N	Y	N	N
5	IDLE IMMEDIATE	95h,E1h	N	N	N	N	Y	N	N
6	INITIALIZE DEVICE PARAMETERS	91h	N	Y	N	N	Y	Y	N
7	NOP	00h	N	N	N	N	Y	N	N
8	READ BUFFER	E4h	N	N	N	N	Y	N	N
9	READ DMA	C8h,C9h	N	Y	Y	Y	Y	Y	Y
10	READ MULTIPLE	C4h	N	Y	Y	Y	Y	Y	Y
11	READ NATIVE MAX ADDRESS	F8h	N	N	N	N	Y	N	Y
12	READ LONG SECTOR	22h,23h	N	N	Y	Y	Y	Y	Y
13	READ SECTOR(S)	20h,21h	N	Y	Y	Y	Y	Y	Y
14	READ VERIFY SECTOR(S)	40h,41h	N	Y	Y	Y	Y	Y	Y
15	RECALIBRATE	1Xh	N	N	N	N	Y	N	N
16	SECURITY DISABLE PASSWORD	F6h	N	N	N	N	Y	N	N
17	SECURITY ERASE PREPARE	F3h	N	N	N	N	Y	N	N
18	SECURITY ERASE UNIT	F4h	N	N	N	N	Y	N	N
19	SECURITY FREEZE LOCK	F5h	N	N	N	N	Y	N	N
20	SECURITY SET PASSWORD	F1h	N	N	N	N	Y	N	N
21	SECURITY UNLOCK	F2h	N	N	N	N	Y	N	N
22	SEEK	7Xh	N	N	Y	Y	Y	Y	Y
23	SET FEATURE	EFh	Y	Y	Y	Y	Y	Y	N
24	SET MULTIPLE	C6h	N	Y	N	N	Y	N	N
25	SLEEP	99h,E6h	N	N	N	N	Y	N	N
26	SMART ENABLE/DISABLE AUTO SAVE	B0h	D2h	Y	N	Y	Y	N	N
27	SMART ENABLE OPERATION	B0h	D8h	N	N	Y	Y	N	N
28	SMART DISABLE OPERATION	B0h	D9h	N	N	Y	Y	N	N
29	SMART RETURN STATUS	B0h	DAh	N	N	Y	Y	N	N
30	STANDBY	96h,E2h	N	N	N	N	Y	N	N
31	STANDBY IMMEDIATE	94h,E0h	N	N	N	N	Y	N	N
32	WRITE BUFFER	E8h	N	N	N	N	Y	N	N
33	Write DMA	CAh,CBh	N	Y	Y	Y	Y	Y	Y
34	Write Multiple	C5h	N	Y	Y	Y	Y	Y	Y
35	Write Long Sector	32h,33h	N	N	Y	Y	Y	Y	Y
36	Write Sector(s)	30h,31h	N	Y	Y	Y	Y	Y	Y
37	Write Verify	3Ch	N	Y	Y	Y	Y	Y	Y

Note : FR: Feature Register
SC: Sector Count registers
SN: Sector Number register
CY: Cylinder Low/High register
DR: Device bit of Device/Head register
HD: Head No. (3 to 0) of Device/Head register
NH: No. of Heads
LBA: Logical Block Address
Y: Setup
N: Not setup

[Command Set Descriptions]

1. CHECK POWER MODE (code: E5h);
This command checks the power mode.

2. EXECUTE DEVICE DIAGNOSTIC (code: 90h);
This command performs the internal diagnostic tests implemented by the module.

3. IDENTIFY DEVICE (code: ECh);
The IDENTIFY DEVICE command enables the host to receive parameter information from the module.

4. IDLE (code: 97h or E3h);
This command allows the host to place the module in the Idle mode and also set the Standby timer. H_INTRQ_P may be asserted even through the module may not have fully transitioned to Idle mode. If the Sector Count register is non-"0", then the Standby timer shall be enabled. The value in the Sector Count register shall be used to determine the time programmed into the Standby timer. If the Sector Count register is "0" then the Standby timer is disabled.

5. IDLE IMMEDIATE (code: 95h or E1h);
This command causes the module to set BSY, enter the Idle (Read) mode, clear BSY and generate an interrupt.

6. INITIALIZE DEVICE PARAMETERS (code: 91h);
This command enables the host to set the number of sectors per track and the number of heads per cylinder.

7. NOP (code: 00h);
If this command is issued, the module respond with command aborted.

8. READ BUFFER (code: E4h);
This command enables the host to read the current contents of the module's sector buffer.

9. READ DMA (code: C8h,C9h);
This command reads from "1" to "256" sectors as specified in the Sector Count register using the DMA data transfer protocol. A sector count of "0" requests "256" sectors transfer. The transfer begins at the sector specified in the Sector Number register.

10. READ MULTIPLE (code: C4h);
This command performs similarly to the READ SECTORS command. Interrupts are not generated on each sector, but on the transfer of a block which contains the number of sectors defined by a Set Multiple commands.

11. READ NATIVE MAX ADDRESS (code: F8h);
This command returns the native maximum address.

12. READ LONG SECTOR (code: 22h, 23h);
This command is provided for compatibility purposes and nearly performs "1" sector READ SECTOR command except that it transfers the data and 4 bytes appended to the sector. These appended 4 bytes are all 0 data.

13. READ SECTOR(S) (code: 20h or 21h);
This command reads from "1" to "256" sectors as specified in the Sector Count register. A sector count of "0" requests "256" sectors transfer. The transfer begins at the sector specified in the Sector Number register.

14. READ VERIFY SECTOR(S) (code: 40h or 41h);
This command is identical to the READ SECTORS command, except that DRQ is never set and no data is transferred to the host.

15. RECALIBRATE (code: 1Xh);
This command return value is select address mode by the host request.

16. SECURITY DISABLE PASSWORD (code: F6h);
This command transfers 512Bytes of data from the host. Table Security Password defines the content of this information.

17. SECURITY ERASE PREPARE (code: F3h);
This command shall be issued immediately before the SECURITY ERASE UNIT command to enable device erasing and unlock. This command prevents accidental erase of the device.

18. SECURITY ERASE UNIT (code: F4h);
This command requests transfer of a single sector of data as form of table SECURITY ERASE UNIT password from the host.
If the password is not match, this command will be reject, the Security Erase Prepare command should be completed immediately prior the Security Erase Unit command.
If Normal Erase mode, the all user data area will be written binary 0, if Enhanced Erase mode, the predetermined data pattern will written to the user data area.

19. SECURITY FREEZE LOCK (code: F5h);
This command sets the device to Frozen mode. After command completion, all other commands that update device lock mode shall be command aborted. Frozen mode shall be disabled by power-off or hardware reset.

20. SECURITY SET PASSWORD (code: F1h);
This command requests a transfer of a single sector of data from the host.

21. SECURITY UNLOCK (code: F2h);
This command requests transfer of a single sector of data from the host.

22. SEEK (code: 7Xh);
This command performs a range check.

23. SET FEATURE (code: EFh);
This command is used by the host to establish parameters that affect the execution of certain device features.

24. SET MULTIPLE MODE (code: C6h);
This command enables the module to perform READ and Write Multiple operations and establishes the block count for these commands.

25. SLEEP (code: 99h or E6h);
This command causes the module to set BSY, enter the Sleep mode, clear BSY and generate an interrupt.

26. SMART ENABLE/DISABLE AUTO SAVE (code: B0h);
This command enables and disables the optional attribute auto save feature of the module.

27. SMART ENABLE OPEARIONS (code: B0h);
This command enables access to all SMART capabilities within the module.

28. SMART DISABLE OPEMTIONS (code: B0h);
This command disables all SMART capabilities within the module.

29. SMART RETURN STATUS (code: B0h);
This command causes the module return the reliability status of the module to the host.

30. STANDBY (code: 96h or E2h);
This command causes the module to set BSY, enter the Sleep mode (which corresponds to the ATA "Standby" Mode), clear BSY and return the interrupt immediately.

31. STANDBY IMMEDIATE (code: 94h or E0h);
This command causes the module to set BSY, enter the Sleep mode (which corresponds to the ATA Standby Mode), clear BSY and return the interrupt immediately.

32. WRITE BUFFER (code: E8h);
This command enables the host to overwrite contents of the module's sector buffer with any data pattern desired.

33. WRITR DMA (code: CAh or CBh);
This command writes from "1" to "256" sectors as specified in the Sector Count register using the DMA data transfer protocol. A sector count of "0" requests "256" sectors transfer. The transfer begins at the sector specified in the Sector Number register.

34. WRITE MULTIPLE (code: C5h);
This command is similar to the WRITE SECTORS command. Interrupts are not presented on each sector, but on the transfer of a block which contains the number of sectors defined by Set Multiple command.

35. WRITE LONG SECTOR (code: 32h or 33h);
This command is provided for compatibility purposes and nearly performs "1" sector WRITE SECTOR command except that it transfers the data and 4 bytes appended to the sector. These appended 4 bytes are not written on the flash memories.

36. WRITE SECTOR(S) (code: 30h or 31h);
This command writes from "1" to "256" sectors as specified in the Sector Count register. A sector count of "0" requests "256" sectors transfer. The transfer begins at the sector specified in the Sector Number register.

37. WRITE VERIFY (code: 3Ch);
This command is similar to the WRITE SECTOR(S) command, except that each sector is verified before the command is completed.

10. System Power Consumption

(Ta = 0 to 60℃)

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
Iccr	Read current	5V	-	75	-	mA
Iccw	Write current	5V	-	75	-	mA
Ipd	Power down current	5V	-	-	0.4	mA
Iccr	Read current	3.3V	-	55	-	mA
Iccw	Write current	3.3V	-	55	-	mA
Ipd	Power down current	3.3V	-	-	0.3	mA

11. Electrical Specifications

Absolute Maximum Rating

Item	Symbol	Parameter	MIN	MAX	Unit	Remark
1	V_{DD}-V_{SS}	DC Power Supply	-0.3	+5.5	V	
2	V_{IN}	Input Voltage	V_{SS}-0.3	V_{DD}+0.3	V	
3	Ta	Operating Temperature	0	+70	℃	Commercial version
4	Tst	Storage Temperature	-25	+85	℃	Commercial version
5	Ta	Operating Temperature	-40	+85	℃	Extended version
6	Tst	Storage Temperature	-40	+85	℃	Extended version

Parameter	Symbol	Min	Typ	MAX	Unit
V_{DD} Voltage	V_{DD}	3.135	3.3	3.465	V
		4.5	5.0	5.5	V

12. DC Characters

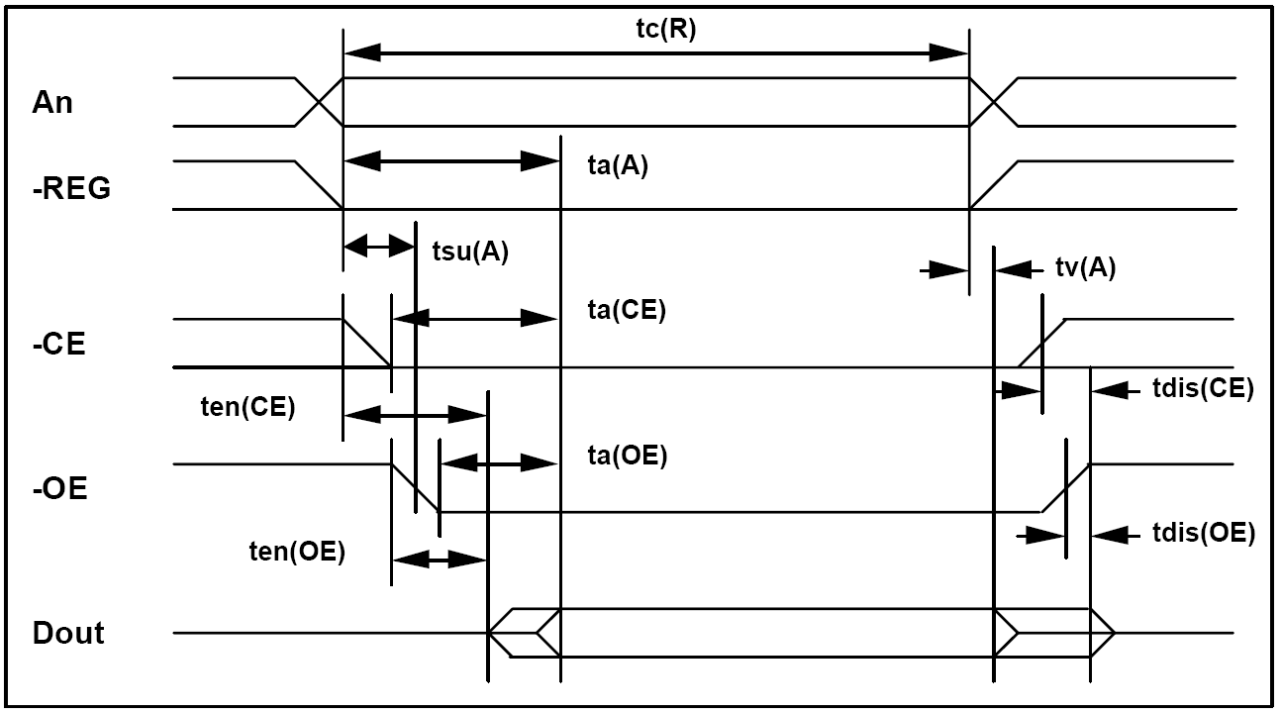
DC characteristics of 5.0V I/O Cells (Host Interface)

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
Vol	Output Low voltage	|Iol| = 4 ~ 32 mA	-	-	0.4	V
Voh	Output High voltage	|Ioh| =4 ~ 32 mA	2.4	-	-	V
Rpu	Input Pull-Up Resistance	PU=high, PD=low	200	300	450	KΩ
Rpd	Input Pull-Down Resistance	PU=high, PD=low	200	300	450	KΩ
Iin	Input Leakage Current	Vin = VCC3I or 0	-10	±1	10	μA
Ioz	Tri-state Output Leakage Current		-10	±1	10	μA

13. AC Characters

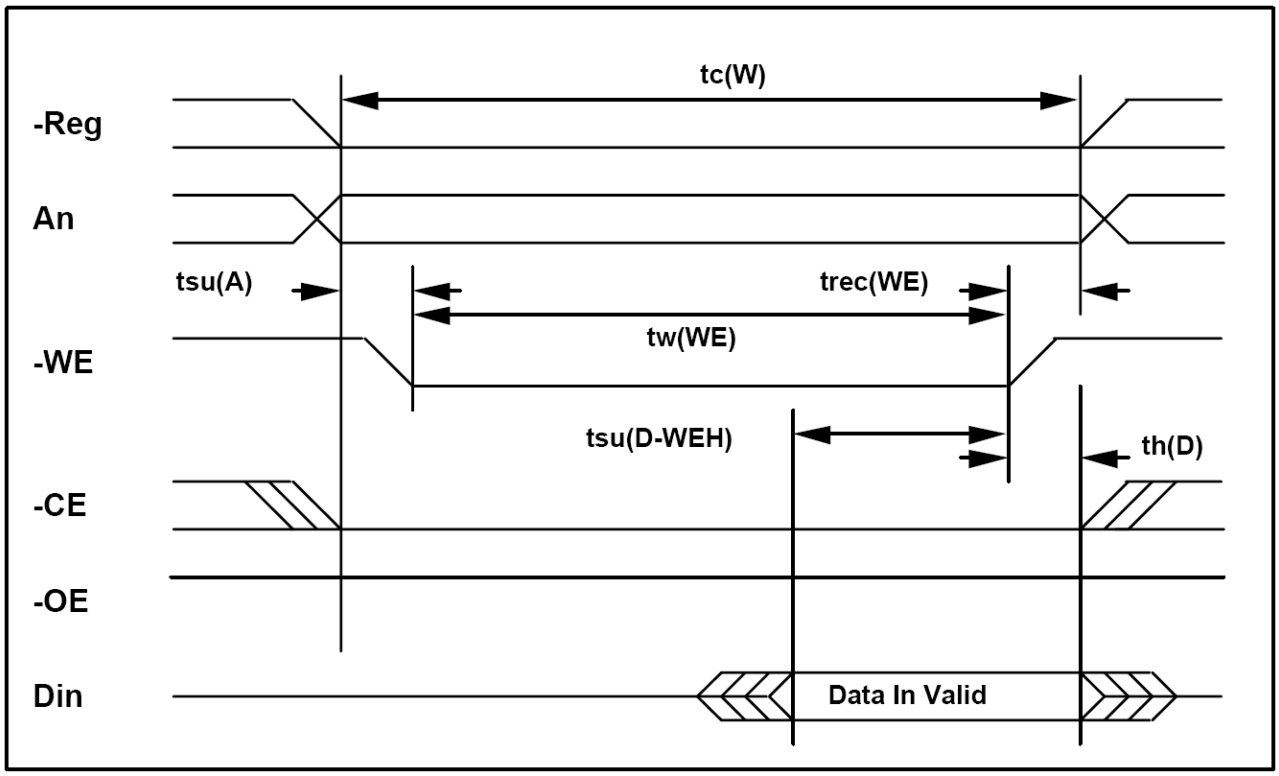
13.1 PCMCIA Interface

[Attribute Memory Read Timing]



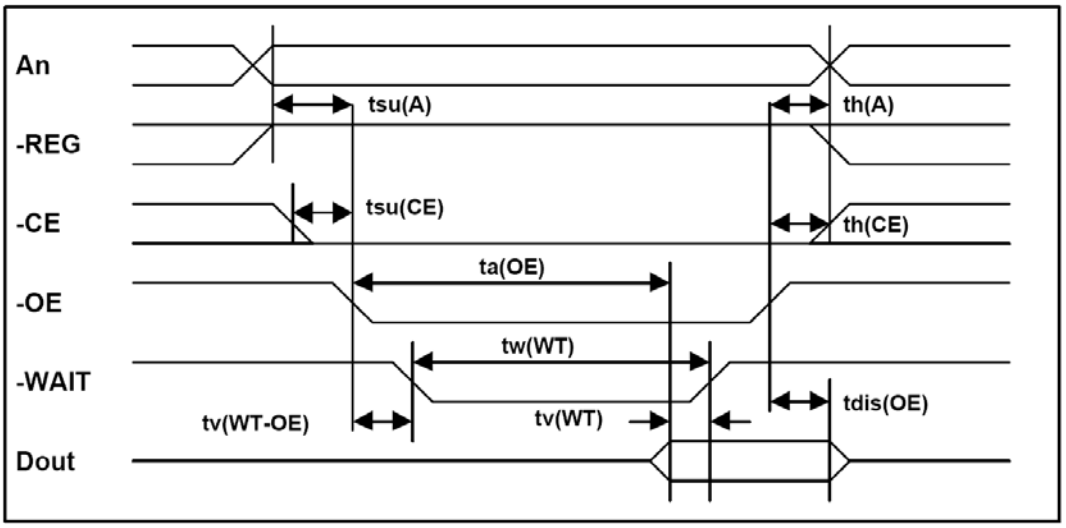
Speed Version			300 ns	
Item	**Symbol**	**IEEE Symbol**	**Min ns.**	**Max ns.**
Read Cycle Time	tc(R)	tAVAV	300	
Address Access Time	ta(A)	tAVQV		300
Card Enable Access Time	ta(CE)	tELQV		300
Output Enable Access Time	ta(OE)	tGLQV		150
Output Disable Time from CE	tdis(CE)	tEHQZ		100
Output Disable Time from OE	tdis(OE)	tGHQZ		100
Address Setup Time	tsu (A)	tAVGL	30	
Output Enable Time from CE	ten(CE)	tELQNZ	5	
Output Enable Time from OE	ten(OE)	tGLQNZ	5	
Data Valid from Address Change	tv(A)	tAXQX	0	

[Attribute Memory Write Timing]



Speed Version			250 ns	
Item	**Symbol**	**IEEE Symbol**	**Min ns**	**Max ns**
Write Cycle Time	tc(W)	tAVAV	250	
Write Pulse Width	tw(WE)	tWLWH	150	
Address Setup Time	tsu(A)	tAVWL	30	
Write Recovery Time	trec(WE)	tWMAX	30	
Data Setup Time for WE	tsu(D-WEH)	tDVWH	80	
Data Hold Time	th(D)	tWMDX	30	

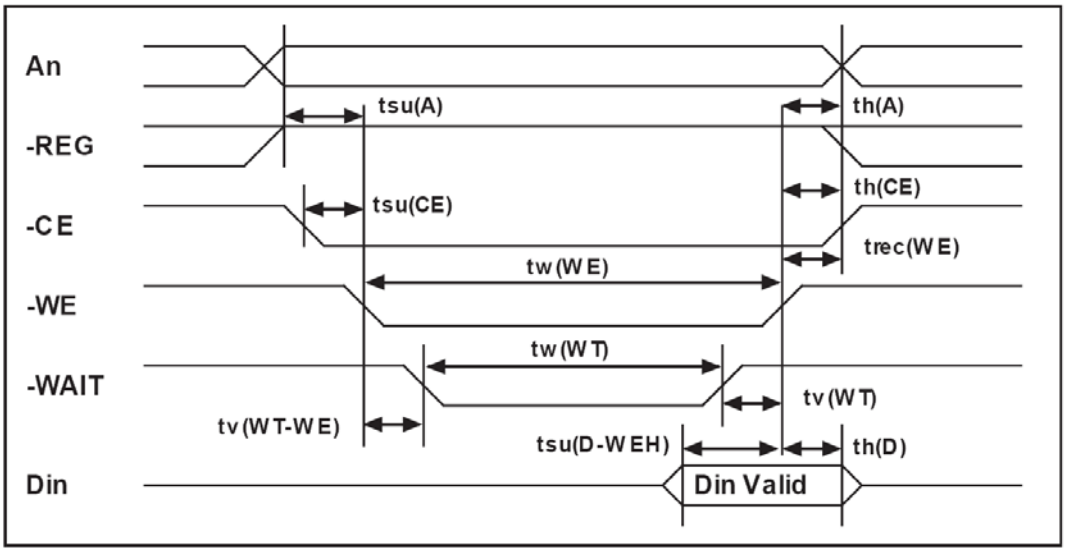
[Common Memory Read Timing]



Cycle Time Mode:			250 ns		120 ns		100 ns		80 ns	
Item	**Symbol**	**IEEE Symbol**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**
Output Enable Access Time	ta(OE)	tGLQV		125		60		50		45
Output Disable Time from OE	tdis(OE)	tGHQZ		100		60		50		45
Address Setup Time	tsu(A)	tAVGL	30		15		10		10	
Address Hold Time	th(A)	tGHAX	20		15		15		10	
CE Setup before OE	tsu(CE)	tELGL	0		0		0		0	
CE Hold following OE	th(CE)	tGHEH	20		15		15		10	
Wait Delay Falling from OE	tv(WT-OE)	tGLWTV		35		35		35		na[1]
Data Setup for Wait Release	tv(WT)	tQVWTH		0		0		0		na[1]
Wait Width Time[2]	tw(WT)	tWTLWTH		350 (3000 for *CF+*)		350 (3000 for *CF+*)		350 (3000 for *CF+*)		na[1]

Notes: 1) –WAIT is not supported in this mode.
2) The maximum load on -WAIT is 1 LSTTL with 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Dout signifies data provided by the CompactFlash Storage Card or CF+ Card to the system. The -WAIT signal may be ignored if the -OE cycle to cycle time is greater than the Wait Width time. The Max Wait Width time can be determined from the Card Information Structure. The Wait Width time meets the PCMCIA specification of 12µs but is intentionally less in this specification.

[Common Memory Write Timing]

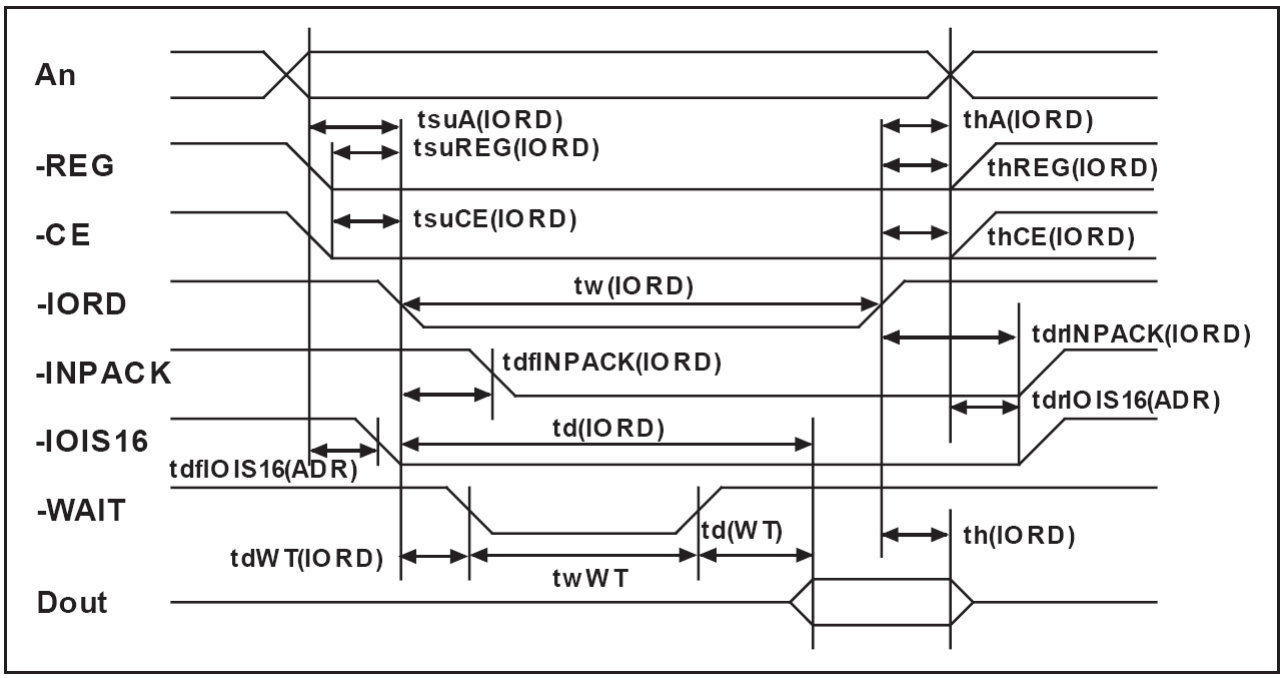


Cycle Time Mode:			250 ns		120 ns		100 ns		80 ns	
Item	**Symbol**	**IEEE Symbol**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**
Data Setup before WE	tsu (D-WEH)	tDVWH	80		50		40		30	
Data Hold following WE	th(D)	tWMDX	30		15		10		10	
WE Pulse Width	tw(WE)	tWLWH	150		70		60		55	
Address Setup Time	tsu(A)	tAVWL	30		15		10		10	
CE Setup before WE	tsu(CE)	tELWL	0		0		0		0	
Write Recovery Time	trec(WE)	tWMAX	30		15		15		15	
Address Hold Time	th(A)	tGHAX	20		15		15		15	
CE Hold following WE	th(CE)	tGHEH	20		15		15		10	
Wait Delay Falling from WE	tv (WT-WE)	tWLWTV		35		35		35		na[1]
WE High from Wait Release	tv(WT)	tWTHWH	0		0		0		na[1]	
Wait Width Time[2]	tw (WT)	tWTLWTH		350 (3000 for *CF+*)		350 (3000 for *CF+*)		350 (3000 for *CF+*)		na[1]

Notes: 1) –WAIT is not supported in this mode.

2) The maximum load on -WAIT is 1 LSTTL with 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Din signifies data provided by the system to the CompactFlash Storage Card. The -WAIT signal may be ignored if the -WE cycle to cycle time is greater than the Wait Width time. The Max Wait Width time can be determined from the Card Information Structure. The Wait Width time meets the PCMCIA specification of 12µs but is intentionally less in this specification.

[I/O Read Timing]



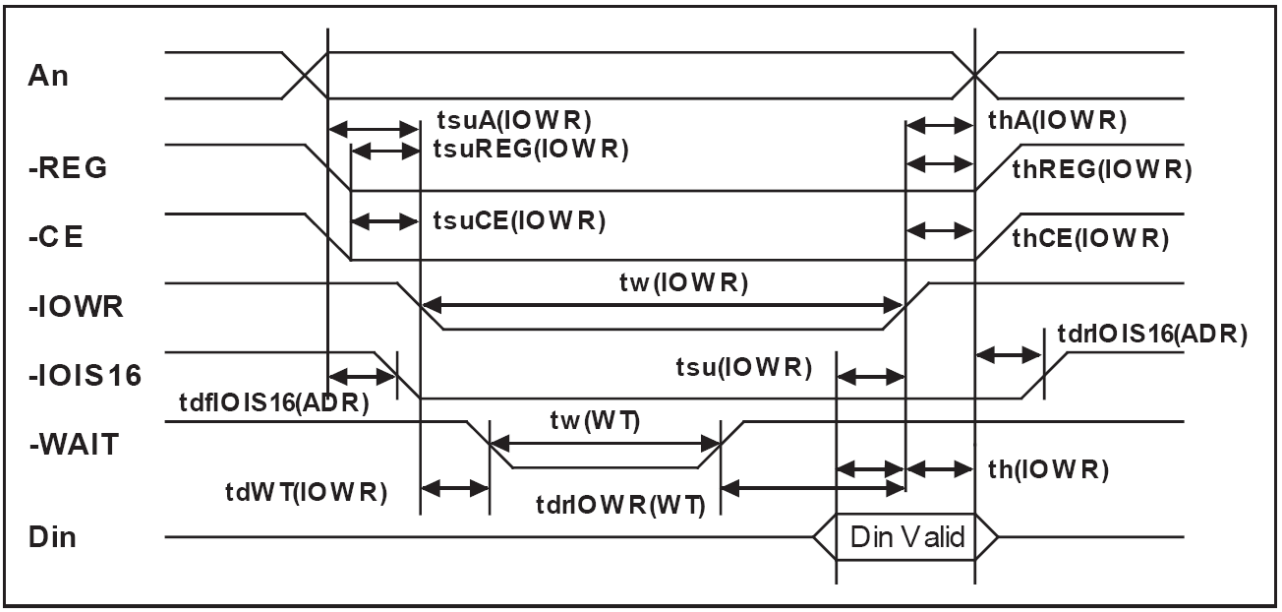
Cycle Time Mode:			250 ns		120 ns		100 ns		80 ns	
Item	**Symbol**	**IEEE Symbol**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**
Data Delay after IORD	td(IORD)	tIGLQV		100		50		50		45
Data Hold following IORD	th(IORD)	tIGHQX	0		5		5		5	
IORD Width Time	tw(IORD)	tIGLIGH	165		70		65		55	
Address Setup before IORD	tsuA(IORD)	tAVIGL	70		25		25		15	
Address Hold following IORD	thA(IORD)	tIGHAX	20		10		10		10	
CE Setup before IORD	tsuCE(IORD)	tELIGL	5		5		5		5	
CE Hold following IORD	thCE(IORD)	tIGHEH	20		10		10		10	
REG Setup before IORD	tsuREG (IORD)	tRGLIGL	5		5		5		5	
REG Hold following IORD	thREG (IORD)	tIGHRGH	0		0		0		0	
INPACK Delay Falling from IORD[3]	tdfINPACK (IORD)	tIGLIAL	0	45	0	na[1]	0	na[1]	0	na[1]
INPACK Delay Rising from IORD[3]	tdrINPACK (IORD)	tIGHIAH		45		na[1]		na[1]		na[1]
IOIS16 Delay Falling from Address[3]	tdfIOIS16 (ADR)	tAVISL		35		na[1]		na[1]		na[1]
IOIS16 Delay Rising from Address[3]	tdrIOIS16 (ADR)	tAVISH		35		na[1]		na[1]		na[1]
Wait Delay Falling from IORD[3]	tdWT(IORD)	tIGLWTL		35		35		35		na[2]
Data Delay from Wait Rising[3]	td(WT)	tWTHQV		0		0		0		na[2]
Wait Width Time[3]	tw(WT)	tWTLWTH		350 (3000 for *CF+*)		350 (3000 for *CF+*)		350 (3000 for *CF+*)		na[2]

Notes:1) -IOIS16 and -INPACK are not supported in this mode.

2) -WAIT is not supported in this mode.

3) Maximum load on -WAIT, -INPACK and -IOIS16 is 1 LSTTL with 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Minimum time from -WAIT high to -IORD high is 0 nsec, but minimum -IORD width shall still be met. Dout signifies data provided by the CompactFlash Storage Card or CF+ Card to the system. Wait Width time meets PCMCIA specification of 12µs but is intentionally less in this spec.

[I/O Write Timing]



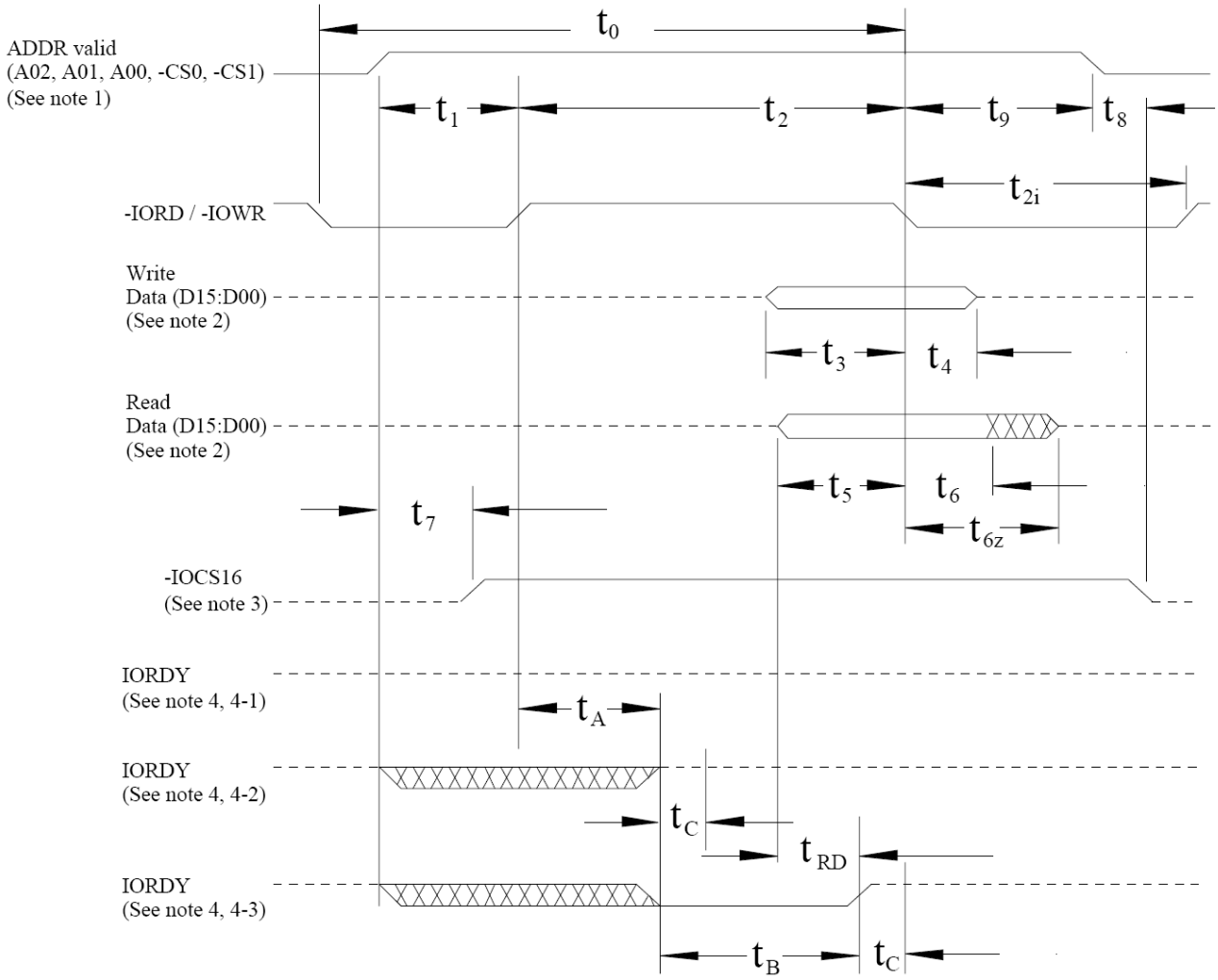
Cycle Time Mode:			255 ns		120 ns		100 ns		80 ns	
Item	**Symbol**	**IEEE Symbol**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**
Data Setup before IOWR	tsu(IOWR)	tDVIWH	60		20		20		15	
Data Hold following IOWR	th(IOWR)	tIWHDX	30		10		5		5	
IOWR Width Time	tw(IOWR)	tIWLIWH	165		70		65		55	
Address Setup before IOWR	tsuA(IOWR)	tAVIWL	70		25		25		15	
Address Hold following IOWR	thA(IOWR)	tIWHAX	20		20		10		10	
CE Setup before IOWR	tsuCE (IOWR)	tELIWL	5		5		5		5	
CE Hold following IOWR	thCE (IOWR)	tIWHEH	20		20		10		10	
REG Setup before IOWR	tsuREG (IOWR)	tRGLIWL	5		5		5		5	
REG Hold following IOWR	thREG (IOWR)	tIWHRGH	0		0		0		0	
IOIS16 Delay Falling from Address[3]	tdfIOIS16 (ADR)	tAVISL		35		na[1]		na[1]		na[1]
IOIS16 Delay Rising from Address[3]	tdrIOIS16 (ADR)	tAVISH		35		na[1]		na[1]		na[1]
Wait Delay Falling from IOWR[3]	tdWT(IOWR)	tIWLWTL		35		35		35		na[2]
IOWR high from Wait high[3]	tdrIOWR (WT)	tWTJIWH	0		0		0		na[2]	
Wait Width Time[3]	tw(WT)	tWTLWTH		350 (3000 for *CF*+)		350 (3000 for *CF*+)		350 (3000 for *CF*+)		na[2]

Notes: 1) -IOIS16 and -INPACK are not supported in this mode.

2) -WAIT is not supported in this mode.

3) The maximum load on -WAIT, -INPACK, and -IOIS16 is 1 LSTTL with 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Minimum time from -WAIT high to -IOWR high is 0 nsec, but minimum -IOWR width shall still be met. Din signifies data provided by the system to the CompactFlash Storage Card or CF+ Card. The Wait Width time meets the PCMCIA specification of 12 µs but is intentionally less in this specification.

13.2 IDE Interface Timing (PIO Mode)



Notes:
(1) Device address consists of -CS0, -CS1, and A[02::00]
(2) Data consists of D[15::00] (16-bit) or D[07::00] (8 bit)
(3) -IOCS16 is shown for PIO modes 0, 1 and 2. For other modes, this signal is ignored.
(4) The negation of IORDY by the device is used to extend the PIO cycle. The determination of whether the cycle is to be extended is made by the host after tA from the assertion of -IORD or -IOWR. The assertion and negation of IORDY is described in the following three cases:
(4-1) Device never negates IORDY: No wait is generated.
(4-2) Device starts to drive IORDY low before tA, but causes IORDY to be asserted before tA: No wait generated.
(4-3) Device drives IORDY low before tA: wait generated. The cycle completes after IORDY is reasserted. For cycles where a wait is generated and -IORD is asserted, the device shall place read data on D15-D00 for tRD before causing IORDY to be asserted.

	Item	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Note
t0	Cycle time (min)	600	383	240	180	120	100	80	1
t1	Address Valid to -IORD/-IOWR setup (min)	70	50	30	30	25	15	10	
t2	-IORD/-IOWR (min)	165	125	100	80	70	65	55	1
t2	-IORD/-IOWR (min) Register (8 bit)	290	290	290	80	70	65	55	1
t2i	-IORD/-IOWR recovery time (min)	-	-	-	70	25	25	20	1
t3	-IOWR data setup (min)	60	45	30	30	20	20	15	
t4	-IOWR data hold (min)	30	20	15	10	10	5	5	
t5	-IORD data setup (min)	50	35	20	20	20	15	10	
t6	-IORD data hold (min)	5	5	5	5	5	5	5	
t6Z	-IORD data tristate (max)	30	30	30	30	30	20	20	2
t7	Address valid to -IOCS16 assertion (max)	90	50	40	n/a	n/a	n/a	n/a	4
t8	Address valid to -IOCS16 released (max)	60	45	30	n/a	n/a	n/a	n/a	4
t9	-IORD/-IOWR to address valid hold	20	15	10	10	10	10	10	
tRD	Read Data Valid to IORDY active (min), if IORDY initially low after tA	0	0	0	0	0	0	0	

tA	IORDY Setup time	35	35	35	35	35	na[5]	na[5]	3
tB	IORDY Pulse Width (max)	1250	1250	1250	1250	1250	na[5]	na[5]	
tC	IORDY assertion to release (max)	5	5	5	5	5	na[5]	na[5]	

Notes: All timings are in nanoseconds. The maximum load on -IOCS16 is 1 LSTTL with a 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Minimum time from -IORDY high to -IORD high is 0 nsec, but minimum -IORD width shall still be met.

1) t0 is the minimum total cycle time, t2 is the minimum command active time, and t2i is the minimum command recovery time or command inactive time. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t0, t2, and t2i shall be met. The minimum total cycle time requirement is greater than the sum of t2 and t2i. This means a host implementation can lengthen either or both t2 or t2i to ensure that t0 is equal to or greater than the value reported in the device's identify device data. A CompactFlash Storage Card implementation shall support any legal host implementation.

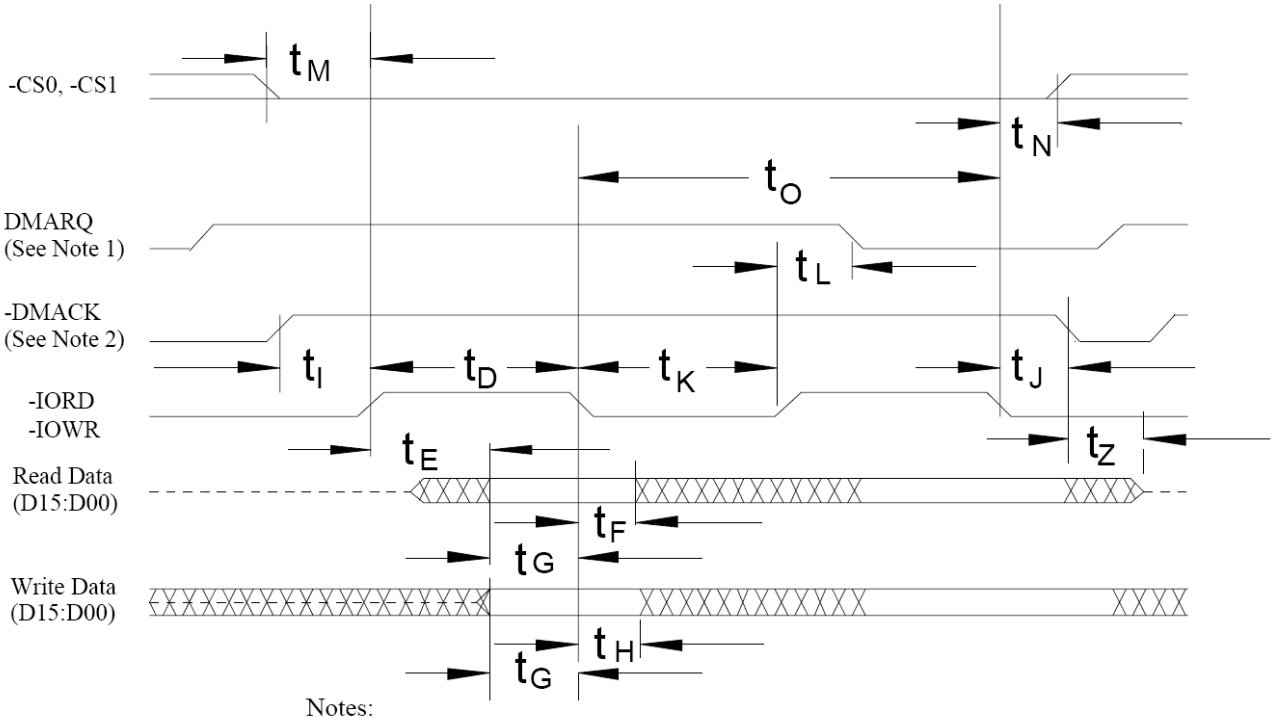
2) This parameter specifies the time from the negation edge of -IORD to the time that the data bus is no longer driven by the CompactFlash Storage Card (tri-state).

3) The delay from the activation of -IORD or -IOWR until the state of IORDY is first sampled. If IORDY is inactive then the host shall wait until IORDY is active before the PIO cycle can be completed. If the CompactFlash Storage Card is not driving IORDY negated at tA after the activation of -IORD or -IOWR, then t5 shall be met and tRD is not applicable. If the CompactFlash Storage Card is driving IORDY negated at the time tA after the activation of -IORD or -IOWR, then tRD shall be met and t5 is not applicable.

4) t7 and t8 apply only to modes 0, 1 and 2. For other modes, this signal is not valid.

5) IORDY is not supported in this mode.

13.3 Multi Word DMA



Notes:

(1) If the Card cannot sustain continuous, minimum cycle time DMA transfers, it may negate DMARQ within the time specified from the start of a DMA transfer cycle to suspend the DMA transfers in progress and reassert the signal at a later time to continue the DMA operation.

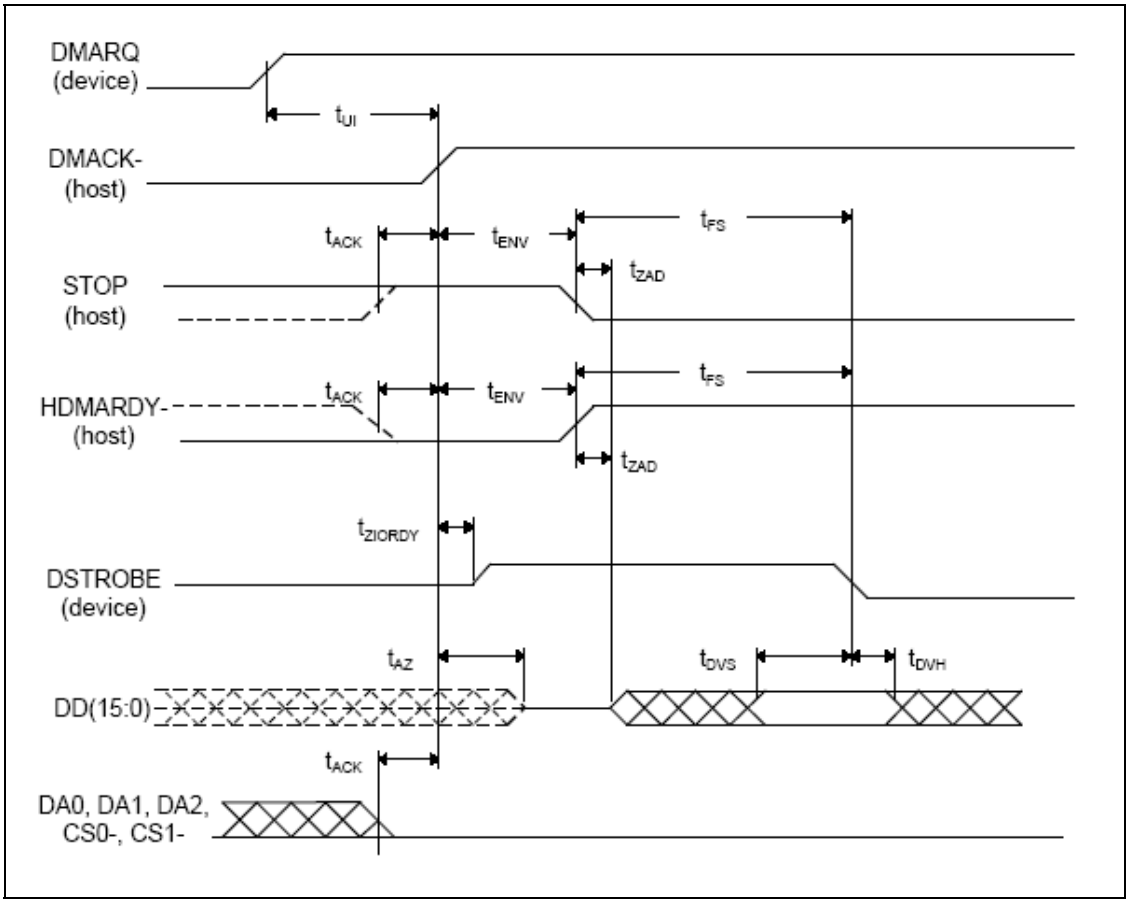
(2) This signal may be negated by the host to suspend the DMA transfer in progress.

ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH. NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

	Item	Mode 0 (ns)	Mode 1 (ns)	Mode 2 (ns)	Mode 3 (ns)	Mode 4 (ns)	Note
t_O	Cycle time (min)	480	150	120	100	80	1
t_D	-IORD / -IOWR asserted width (min)	215	80	70	65	55	1
t_E	-IORD data access (max)	150	60	50	50	45	
t_F	-IORD data hold (min)	5	5	5	5	5	
t_G	-IORD/-IOWR data setup (min)	100	30	20	15	10	
t_H	-IOWR data hold (min)	20	15	10	5	5	
t_I	DMACK to –IORD/-IOWR setup (min)	0	0	0	0	0	
t_J	-IORD / -IOWR to -DMACK hold (min)	20	5	5	5	5	
t_{KR}	-IORD negated width (min)	50	50	25	25	20	1
t_{KW}	-IOWR negated width (min)	215	50	25	25	20	1
t_{LR}	-IORD to DMARQ delay (max)	120	40	35	35	35	
t_{LW}	-IOWR to DMARQ delay (max)	40	40	35	35	35	
t_M	CS(1:0) valid to –IORD / -IOWR	50	30	25	10	5	
t_N	CS(1:0) hold	15	10	10	10	10	
t_Z	-DMACK	20	25	25	25	25	

Notes: 1) t_0 is the minimum total cycle time and t_D is the minimum command active time, while t_{KR} and t_{KW} are the minimum command recovery time or command inactive time for input and output cycles respectively. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t_0, t_D, t_{KR}, and t_{KW} shall be met. The minimum total cycle time requirement is greater than the sum of t_D and t_{KR} or t_{KW}.for input and output cycles respectively. This means a host implementation can lengthen either or both of t_D and either of t_{KR}, and t_{KW} as needed to ensure that t_0 is equal to or greater than the value reported in the device's identify device data. A CompactFlash Storage Card implementation shall support any legal host implementation.

13.4 Ultra DMA



Name	Mode 0 (in ns)		Mode 1 (in ns)		Mode 2 (in ns)		Mode 3 (in ns)		Mode 4 (in ns)		Mode 5 (in ns)		Measurement location.
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$t_{2CYCTYP}$	240		160		120		90		60		40		Sender
t_{CYC}	112		73		54		39		25		16.8		Recipient
t_{2CYC}	230		153		115		86		57		38		Sender
t_{DS}	15.0		10.0		7.0		7.0		5.0		4.0		Recipient
t_{DH}	5.0		5.0		5.0		5.0		5.0		4.6		Recipient
t_{DVS}	70.0		48.0		31.0		20.0		6.7		4.8		Sender
t_{DVH}	6.2		6.2		6.2		6.2		6.2		4.8		Sender
t_{CS}	15.0		10.0		7.0		7.0		5.0		5.0		Device
t_{CH}	5.0		5.0		5.0		5.0		5.0		5.0		Device
t_{CVS}	70.0		48.0		31.0		20.0		6.7		10.0		Host
t_{CVH}	6.2		6.2		6.2		6.2		6.2		10.0		Host
t_{ZFS}	0		0		0		0		0		35		Device
t_{DZFS}	70.0		48.0		31.0		20.0		6.7		25		Sender
t_{FS}		230		200		170		130		120		90	Device
t_{LI}	0	150	0	150	0	150	0	100	0	100	0	75	Note 2
t_{MLI}	20		20		20		20		20		20		Host
t_{UI}	0		0		0		0		0		0		Host
t_{AZ}		10		10		10		10		10		10	Note 3
t_{ZAH}	20		20		20		20		20		20		Host
t_{ZAD}	0		0		0		0		0		0		Device
t_{ENV}	20	70	20	70	20	70	20	55	20	55	20	50	Host
t_{RFS}		75		70		60		60		60		50	Sender
t_{RP}	160		125		100		100		100		85		Recipient
t_{IORDYZ}		20		20		20		20		20		20	Device
t_{ZIORDY}	0		0		0		0		0		0		Device
t_{ACK}	20		20		20		20		20		20		Host
t_{SS}	50		50		50		50		50		50		Sender

NOTES –

1 All signal transitions for a timing parameter shall be measured at the connector specified in the measurement location column. For example, in the case of t_{RFS}, both STROBE and DMARDY- transitions are measured at the sender connector.

2 The parameter t_{LI} shall be measured at the connector of the sender or recipient that is responding to an incoming transition from the recipient or sender respectively. Both the incoming signal and the outgoing response shall be measured at the same connector.

3 The parameter t_{AZ} shall be measured at the connector of the sender or recipient that is releasing the bus.

Notes: 1) The parameters t_{UI}, t_{MLI} (in Figure 36: Ultra DMA Data-In Burst Device Termination Timing and Figure 37: Ultra DMA Data-In Burst Host Termination Timing), and t_{LI} indicate sender-to-recipient or recipient-to-sender interlocks, i.e., one agent (either sender or recipient) is waiting for the other agent to respond with a signal before proceeding. t_{UI} is an unlimited interlock that has no maximum time value. t_{MLI} is a limited time-out that has a defined minimum. t_{LI} is a limited time-out that has a defined maximum.

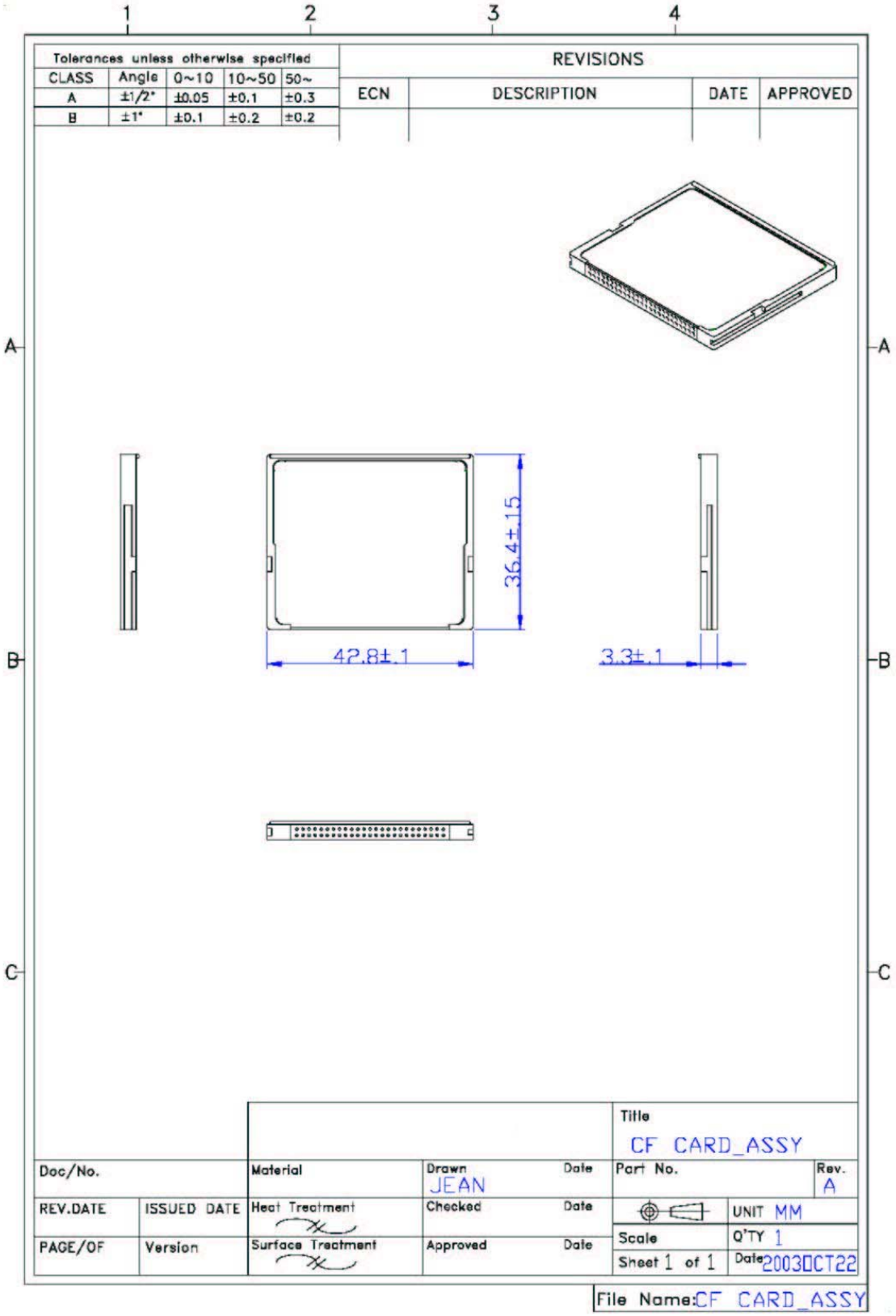
2) 80-conductor cabling (see 4.3.8.4) shall be required in order to meet setup (t_{DS}, t_{CS}) and hold (t_{DH}, t_{CH}) times in modes greater than 2.

3) Timing for t_{DVS}, t_{DVH}, t_{CVS} and t_{CVH} shall be met for lumped capacitive loads of 15 and 40 pF at the connector where the Data and STROBE signals have the same capacitive load value. Due to reflections on the cable, these timing measurements are not valid in a normally functioning system.

4) For all modes the parameter t_{ZIORDY} may be greater than t_{ENV} due to the fact that the host has a pull-up on IORDY- giving it a known state when released.

5) The parameters t_{DS}, and t_{DH} for mode 5 are defined for a recipient at the end of the cable only in a configuration with a single device located at the end of the cable. This could result in the minimum values for t_{DS} and t_{DH} for mode 5 at the middle connector being 3.0 and 3.9 ns respectively.

14. Package Specifications



15. CF Card Capacity

Capacity	Total LBA	
	SLC	MLC
128MB	250880	
256MB	501760	492544
512MB	1002960	984816
1GB	2006928	1969632
2GB	4013856	3940272
4GB	8027712	7880544
8GB	16055424	15761088
16GB	32111856	31522176
32GB		63045360

Appendix: Part Number Table

Product	Advantech PN	Manufacture PN
Advantech SQFlash 1G CF NR, DMA (0~70°C)	SQF-P10S1-1G-CTE	GC7HPF00T61-D000A1
Advantech SQFlash 2G CF NR, DMA (0~70°C)	SQF-P10S2-2G-CTE	GC7HPF00T72-D000A1
Advantech SQFlash 4G CF NR, DMA (0~70°C)	SQF-P10S2-4G-CTE	GC7HPF00T82-D000A1
Advantech SQFlash 8G CF NR, DMA (0~70°C)	SQF-P10S2-8G-CTE	GC7HPF00T92-D000A1
Advantech SQFlash 16G CF NR, DMA (0~70°C)	SQF-P10S2-16G-CTE	GC7HPF00TA4-D000A1
Advantech SQFlash 1G CF NR, DMA (-40~85°C)	SQF-P10S1-1G-ETE	GC7IPF00T61-D000A1
Advantech SQFlash 2G CF NR, DMA (-40~85°C)	SQF-P10S2-2G-ETE	GC7IPF00T72-D000A1
Advantech SQFlash 4G CF NR, DMA (-40~85°C)	SQF-P10S2-4G-ETE	GC7IPF00T82-D000A1
Advantech SQFlash 8G CF NR, DMA (-40~85°C)	SQF-P10S2-8G-ETE	GC7IPF00T92-D000A1
Advantech SQFlash 16G CF NR, DMA (-40~85°C)	SQF-P10S2-16G-ETE	GC7IPF00TA4-D000A1